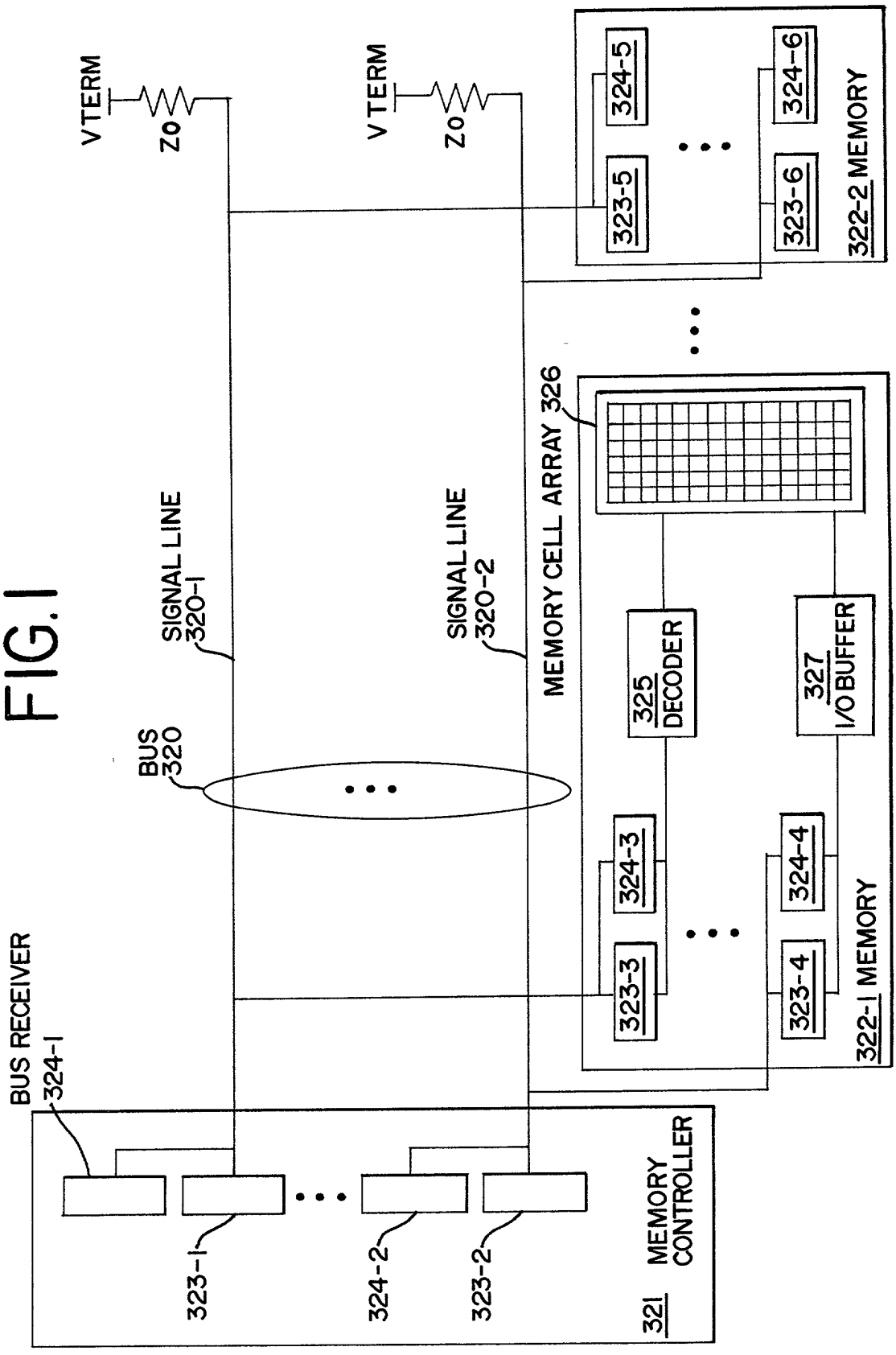

VTERM
Z0
VTERM
Z0
324-5
324-6
323-5
323-6
322-2 MEMORY
SIGNAL LINE
320-1
SIGNAL LINE
320-2
MEMORY CELL ARRAY 326
BUS
320
325
DECODER
327
I/O BUFFER
324-3
324-4
323-3
323-4
322-1 MEMORY
BUS RECEIVER
324-1
323-1
324-2
323-2
321 MEMORY
CONTROLLER

FIG. 1

FIG.2

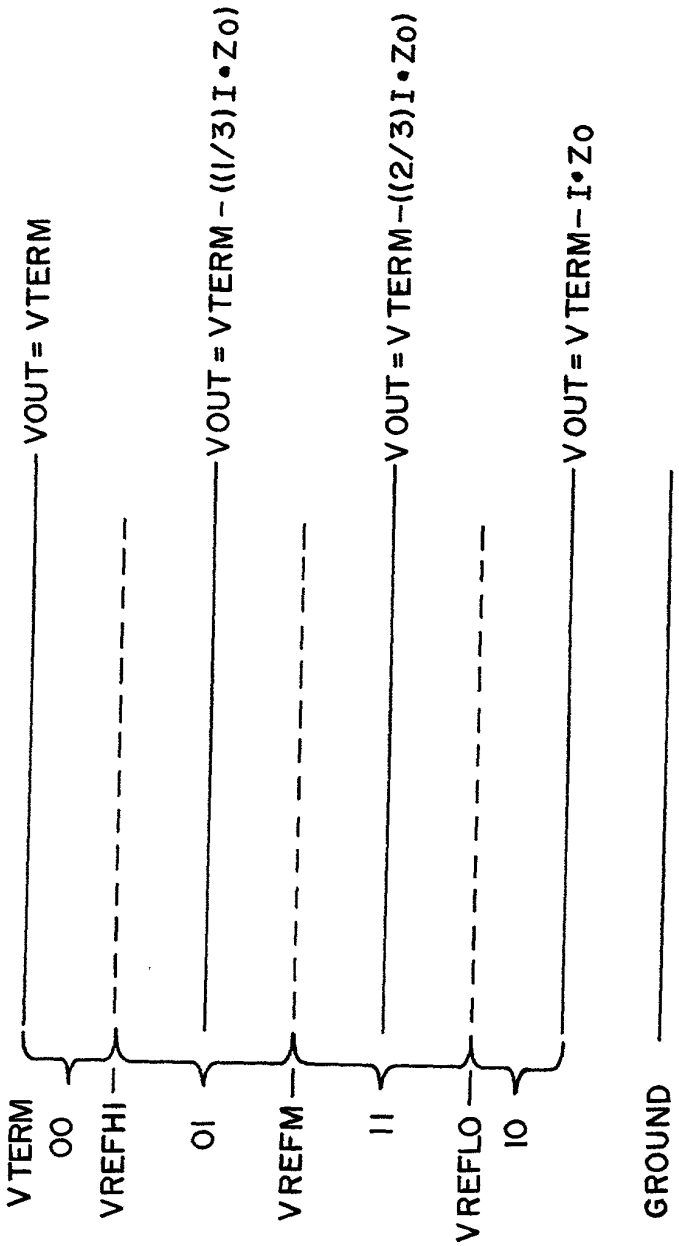


FIG.3A

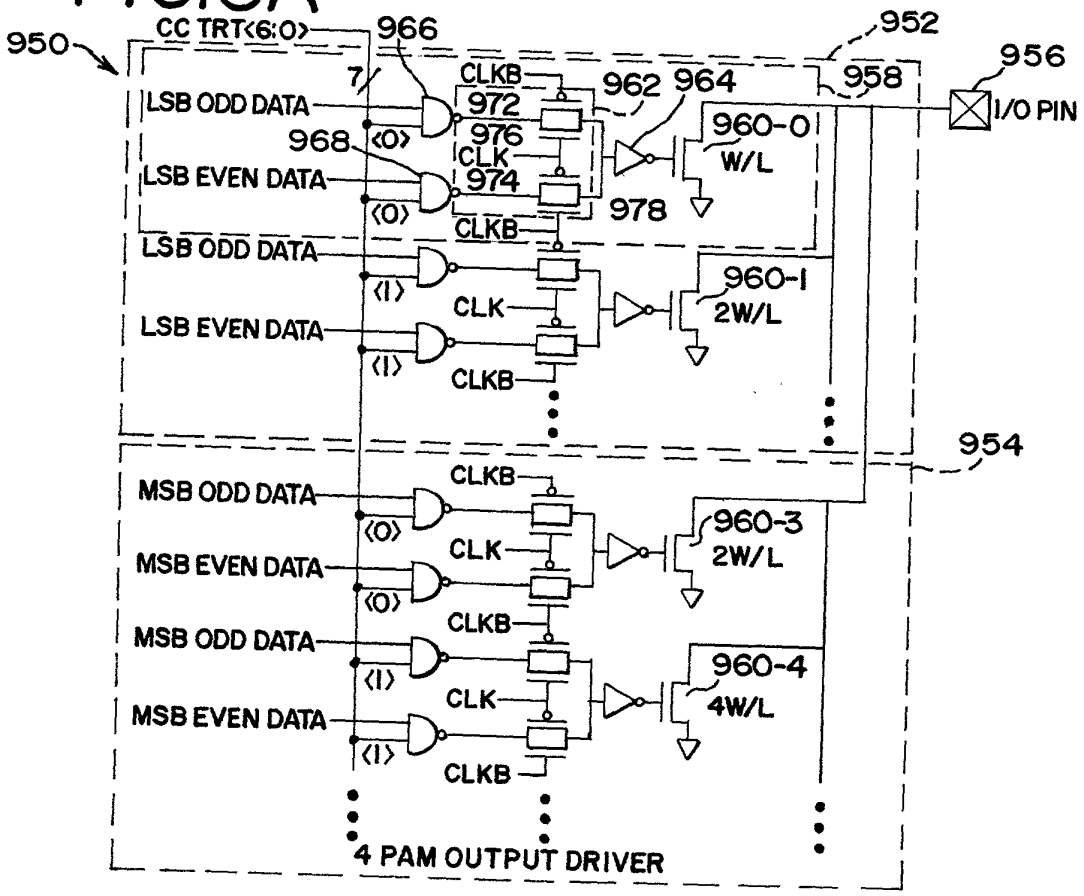

950
CC TRT<6:0>
966
952
956
7
CLKB
962
964
958
I/O PIN
LSB ODD DATA
972
968
<0>
976
CLK
960-0
W/L
LSB EVEN DATA
974
<0>
978
CLKB
LSB ODD DATA
960-1
<1>
CLK
2W/L
LSB EVEN DATA
<1>
CLKB
954
MSB ODD DATA
CLKB
<0>
960-3
CLK
2W/L
MSB EVEN DATA
<0>
CLKB
MSB ODD DATA
960-4
<1>
CLK
4W/L
MSB EVEN DATA
<1>
CLKB
4 PAM OUTPUT DRIVER

FIG.3B

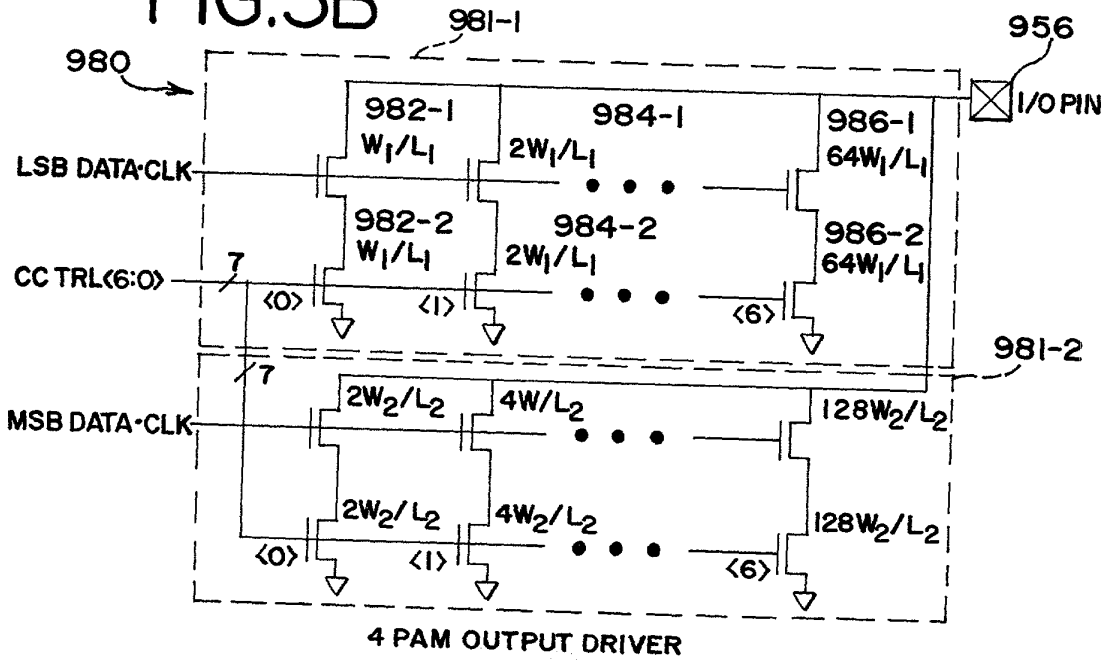

981-1
956
980
I/O PIN
982-1
W1/L1
984-1
2W1/L1
986-1
64W1/L1
LSB DATA·CLK
982-2
W1/L1
984-2
2W1/L1
986-2
64W1/L1
CC TRL<6:0>
7
<0>
<1>
<6>
981-2
7
2W2/L2
4W/L2
128W2/L2
MSB DATA·CLK
2W2/L2
4W2/L2
128W2/L2
<0>
<1>
<6>
4 PAM OUTPUT DRIVER

FIG. 4A

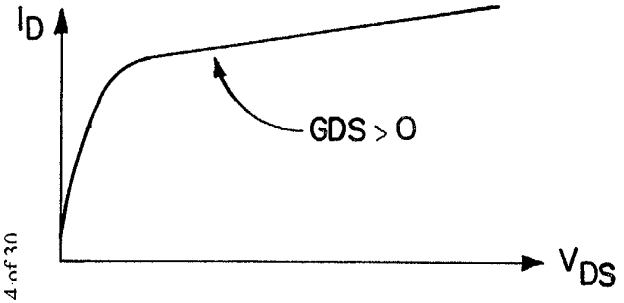


FIG. 4B

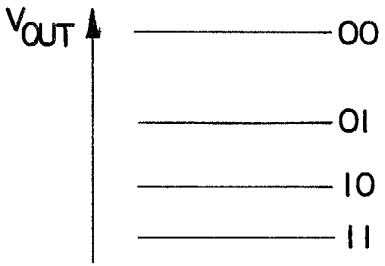


FIG. 4C

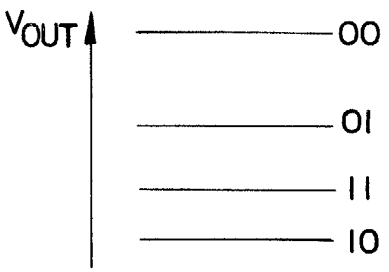
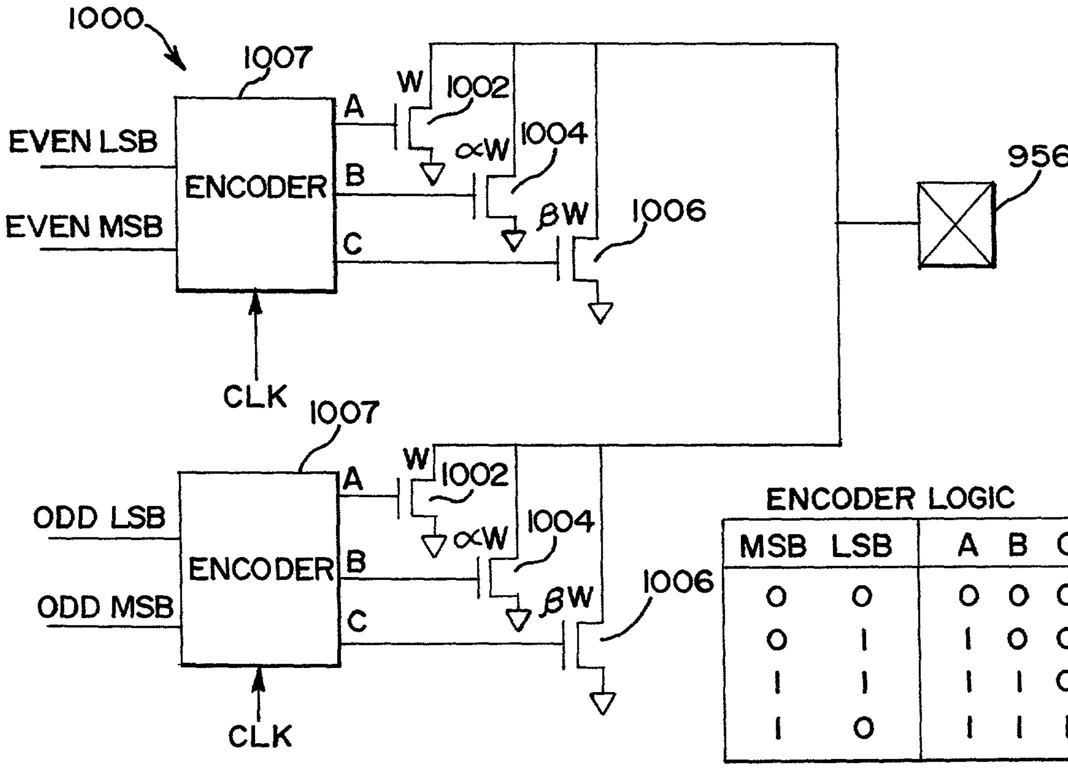


FIG.5A



ENCODER LOGIC

MSB	LSB	A	B	C
0	0	0	0	0
0	1	1	0	0
1	1	1	1	0
1	0	1	1	1

FIG.5B

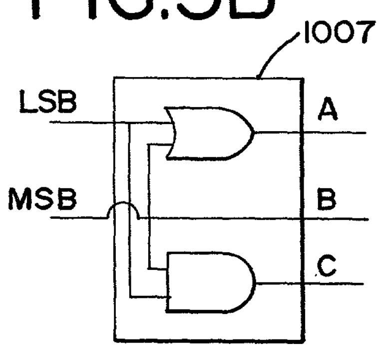


FIG.5C

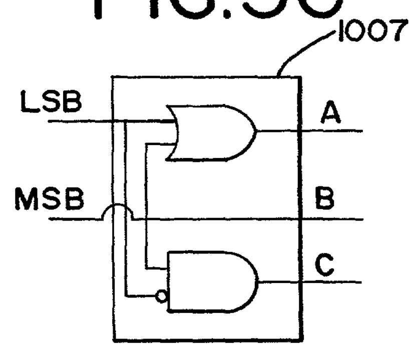
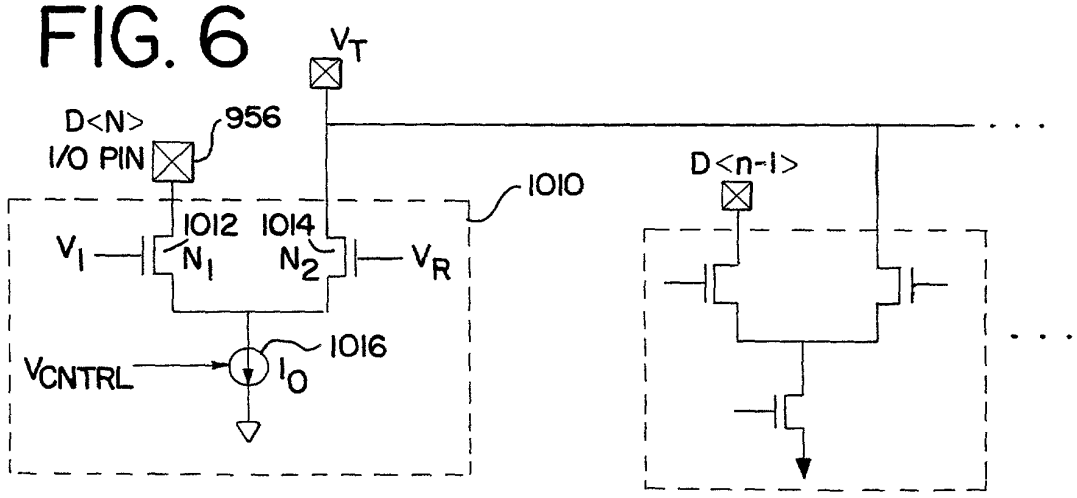


FIG. 6



CIRCUIT TO REDUCE SWITCHING NOISE

FIG. 7

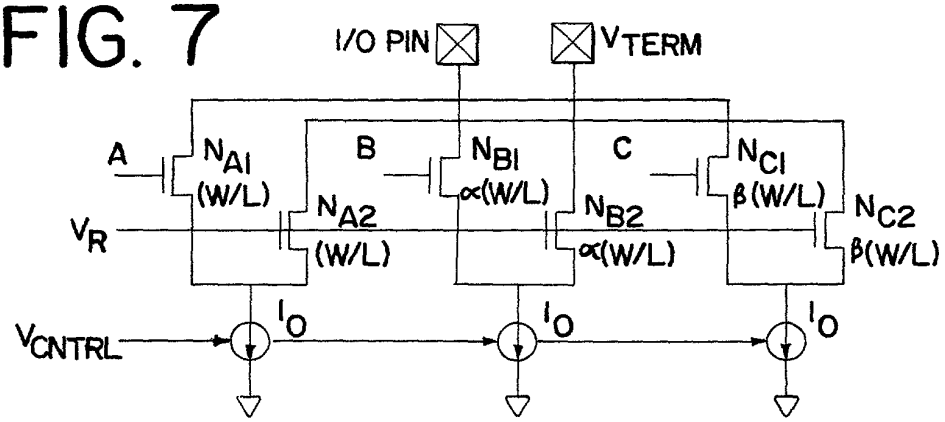
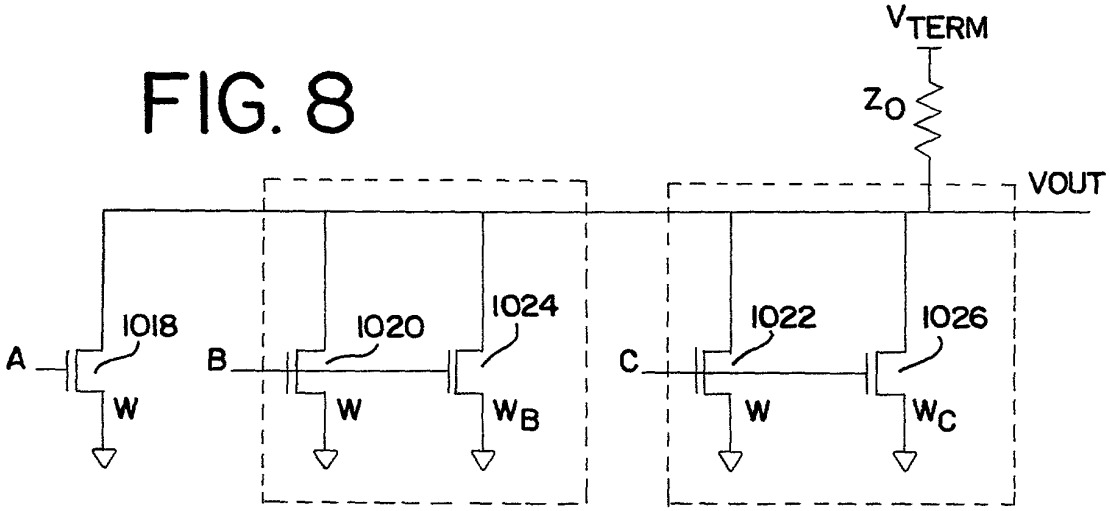
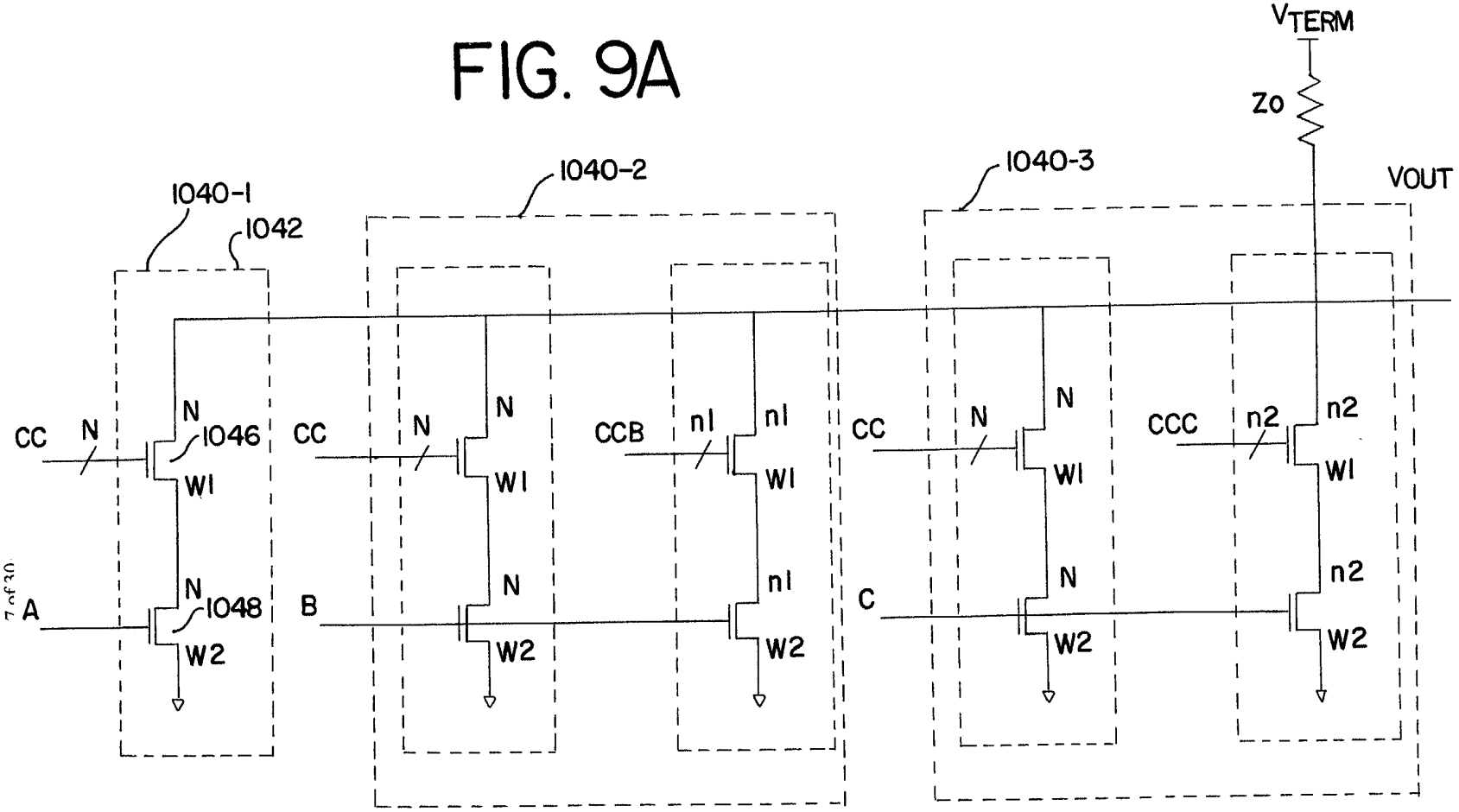


FIG. 8



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER

FIG. 9A



GDS COMPENSATED MULTI-PAM OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 9B

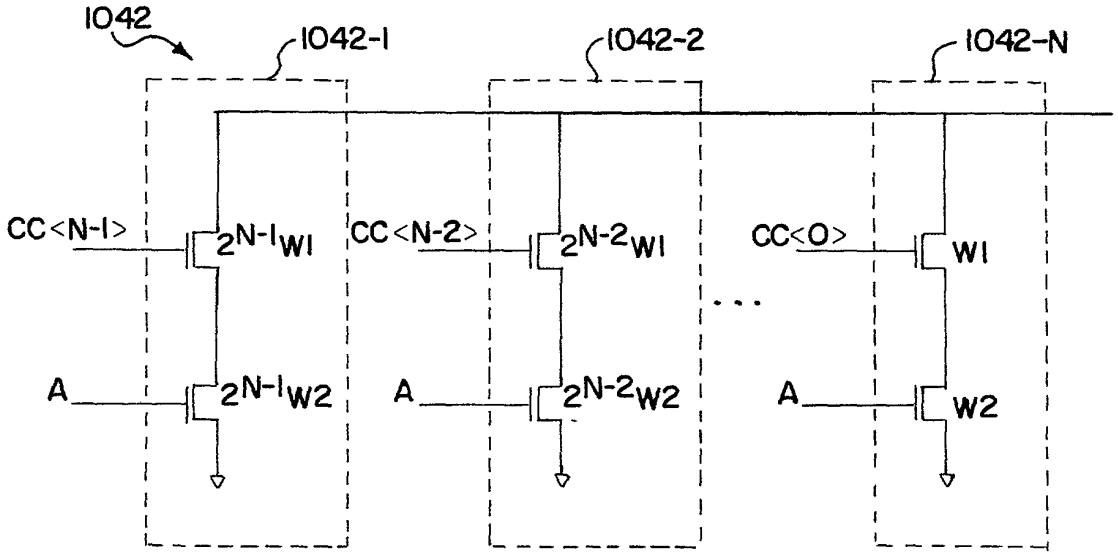


FIG. 9C

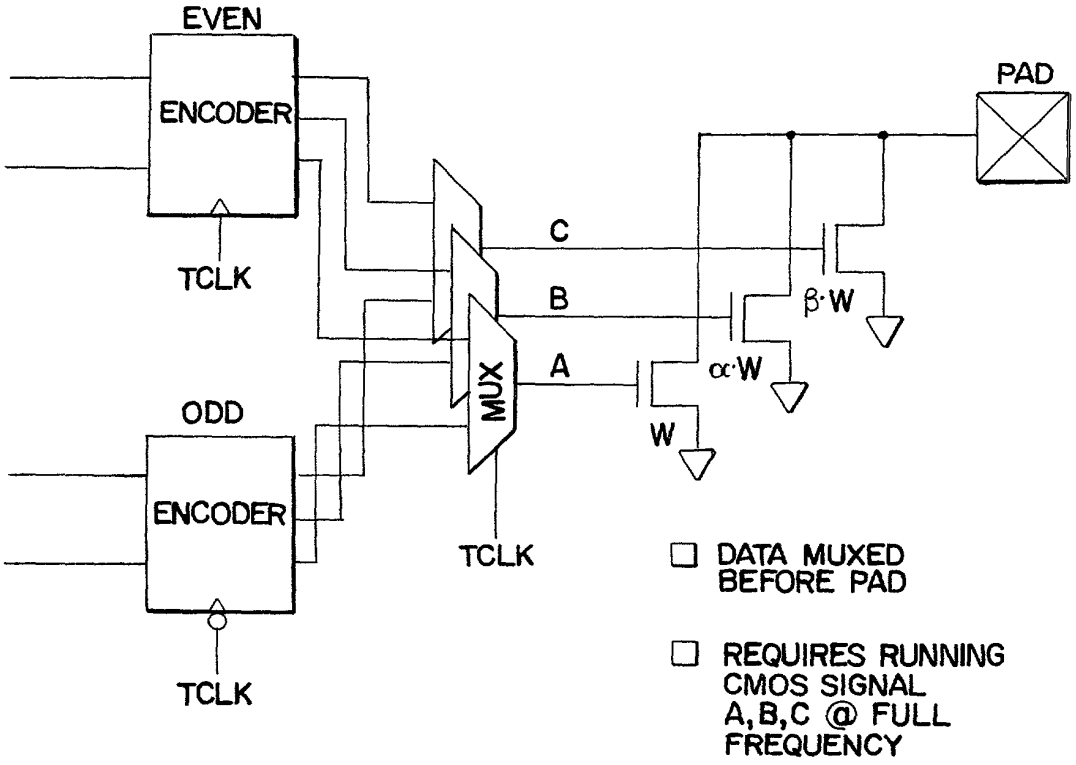
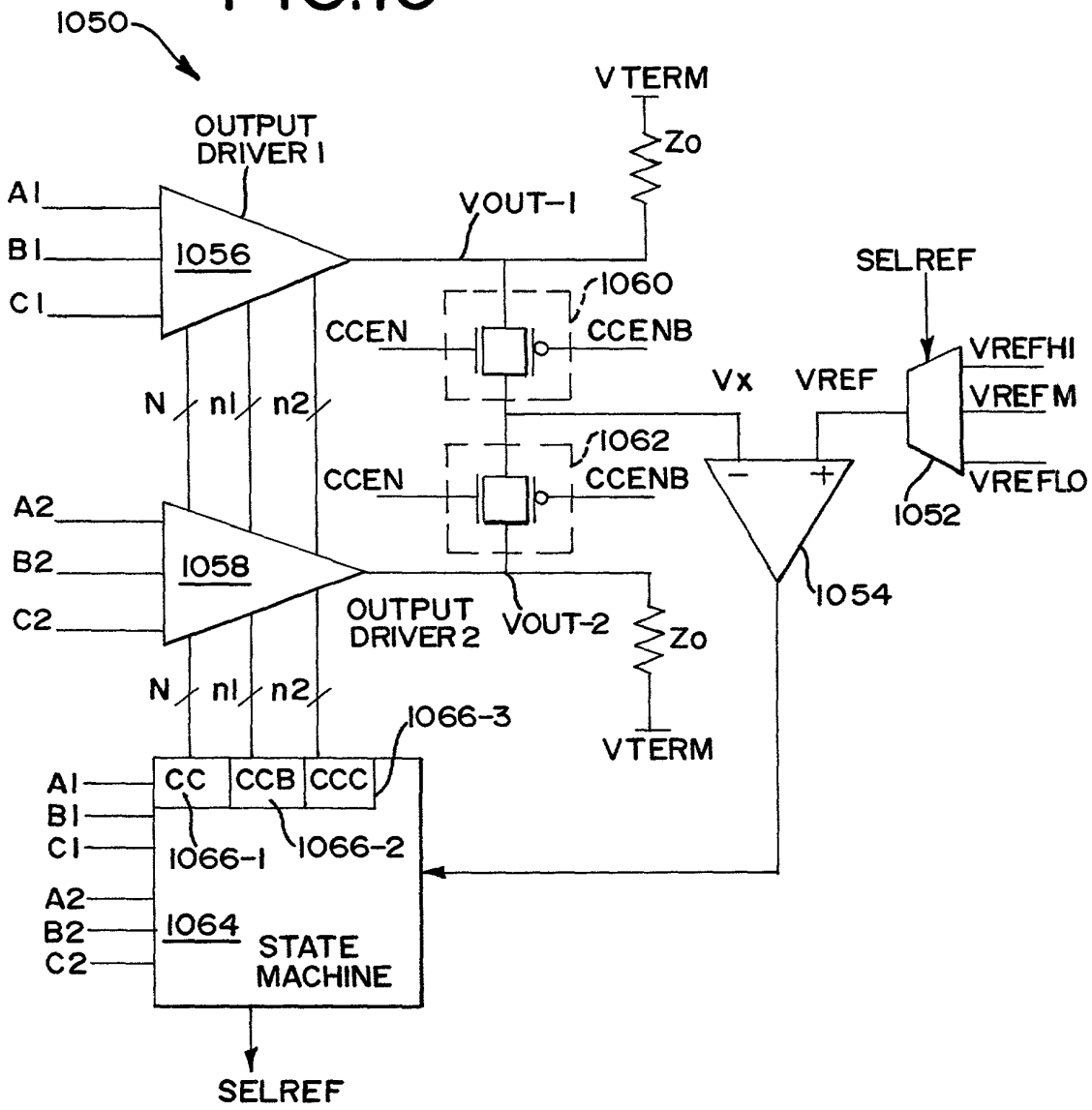
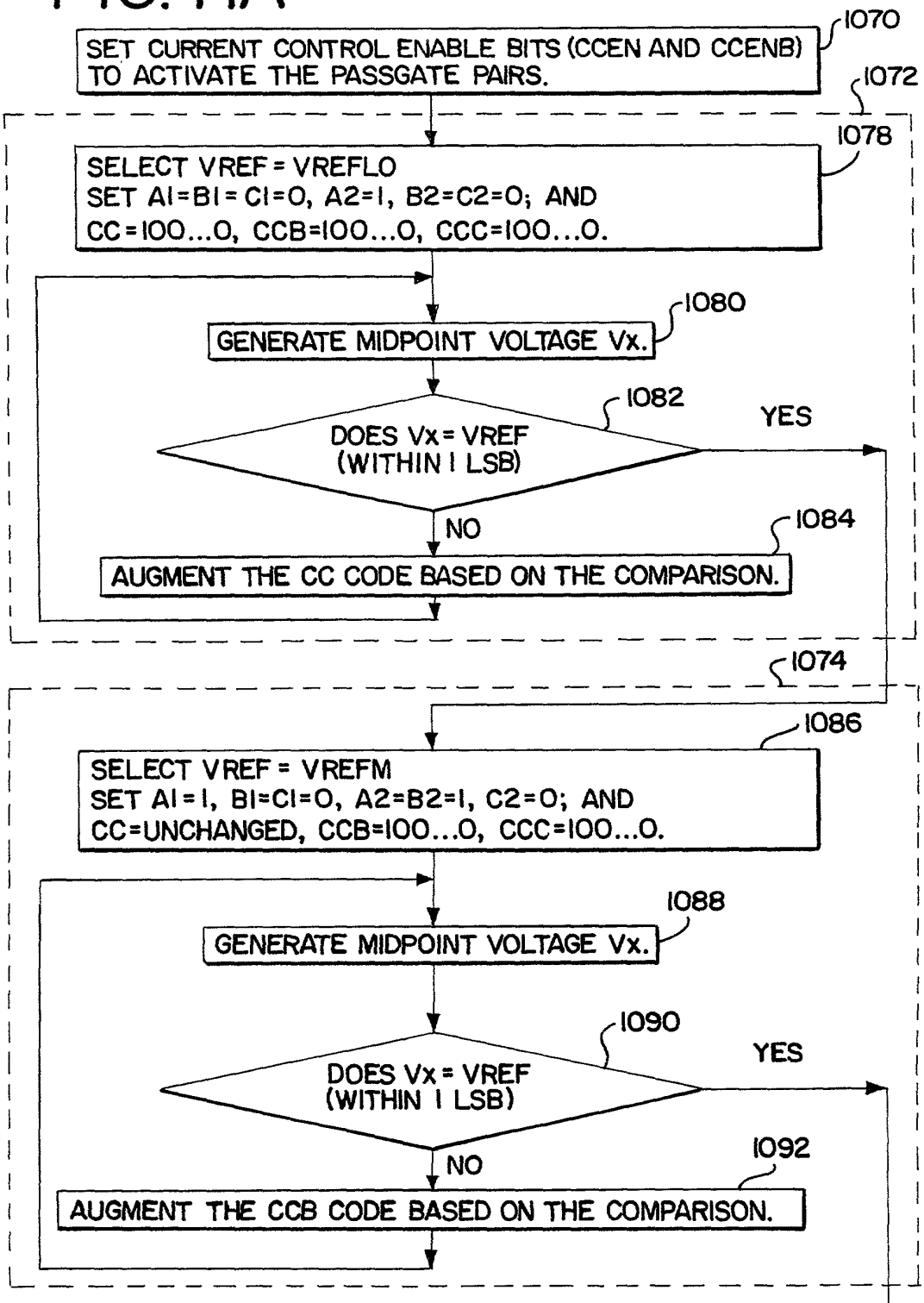


FIG.10



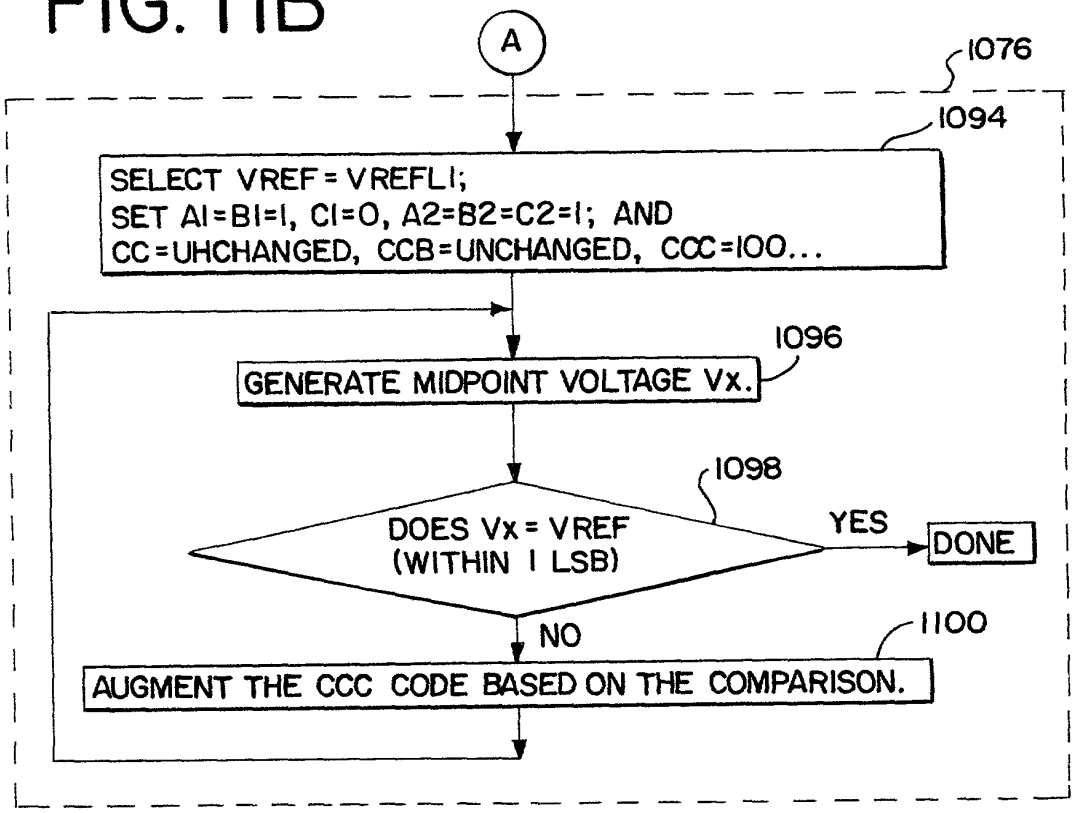
CIRCUIT FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 11A



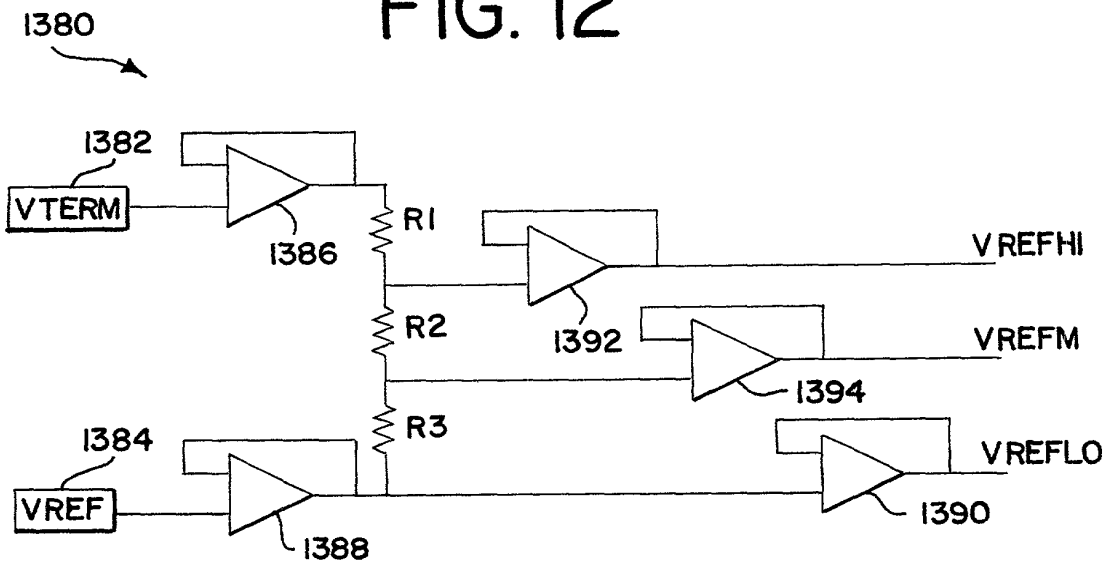
METHOD FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 11B



METHOD FOR CALIBRATING THE GDS COMPENSATED OUTPUT DRIVER WITH CURRENT CONTROL

FIG. 12



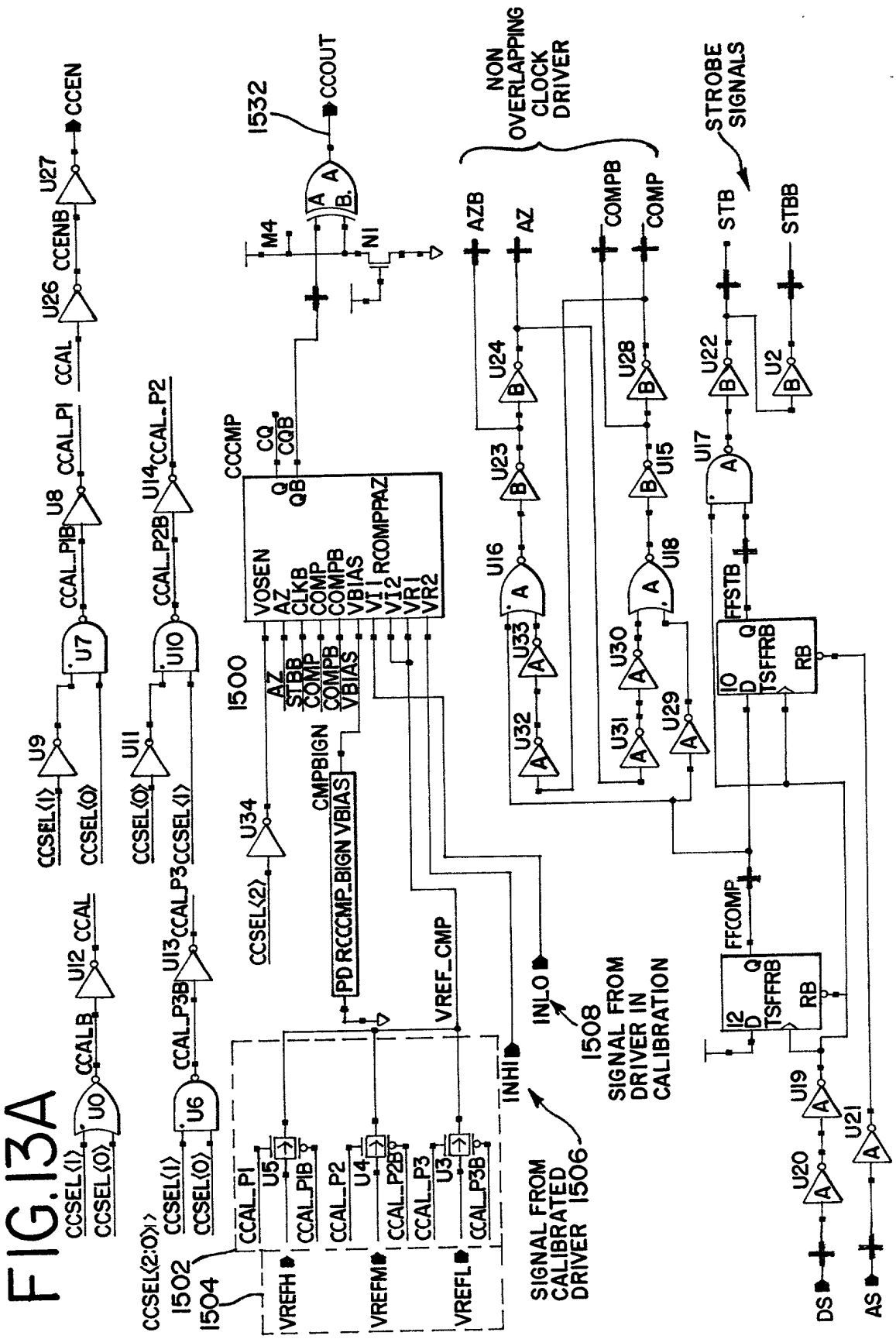

CCSEL<1>
CCSEL<0>
CCALB
U0
U12
CCAL
U9
U7
U8
CCAL_P1B
CCAL_P1
U26
CCENB
U27
CCEN
CCSEL<2:0>
1502
1504
CCSEL<1>
CCSEL<0>
U6
U13
CCAL_P3B
CCAL_P3
U11
U10
U14
CCAL_P2B
CCAL_P2
CCSEL<0>
CCSEL<1>
U34
CCSEL<2>
1500
CCCMP
CQ
COB
Q
QB
VOSEN
AZ
CLKB
COMP
COMPB
VBIAS
VI1
VI2
VR1
VR2
RCOMPPAZ
AZ
STBB
COMP
COMPB
VBIAS
CMPBIGN
PD RCCCMP_BIGN VBIAS
VREF_CMP
1532
CCOUT
M4
NI
INHI
INLO
1508
SIGNAL FROM
DRIVER IN
CALIBRATION
SIGNAL FROM
CALIBRATED
DRIVER 1506
U5
U4
U3
CCAL_P1
CCAL_P1B
CCAL_P2
CCAL_P2B
CCAL_P3
CCAL_P3B
VREFH
VREFM
VREFL
NON
OVERLAPPING
CLOCK
DRIVER
AZB
AZ
COMPB
COMP
U24
U23
U16
U33
U32
U28
U15
U18
U30
U31
U29
STROBE
SIGNALS
STB
STBB
U22
U2
U17
FFSTB
I0
D
Q
TSFFRB
RB
FFCOMP
I2
D
Q
TSFFRB
RB
U19
U20
U21
DS
AS

FIG.13A

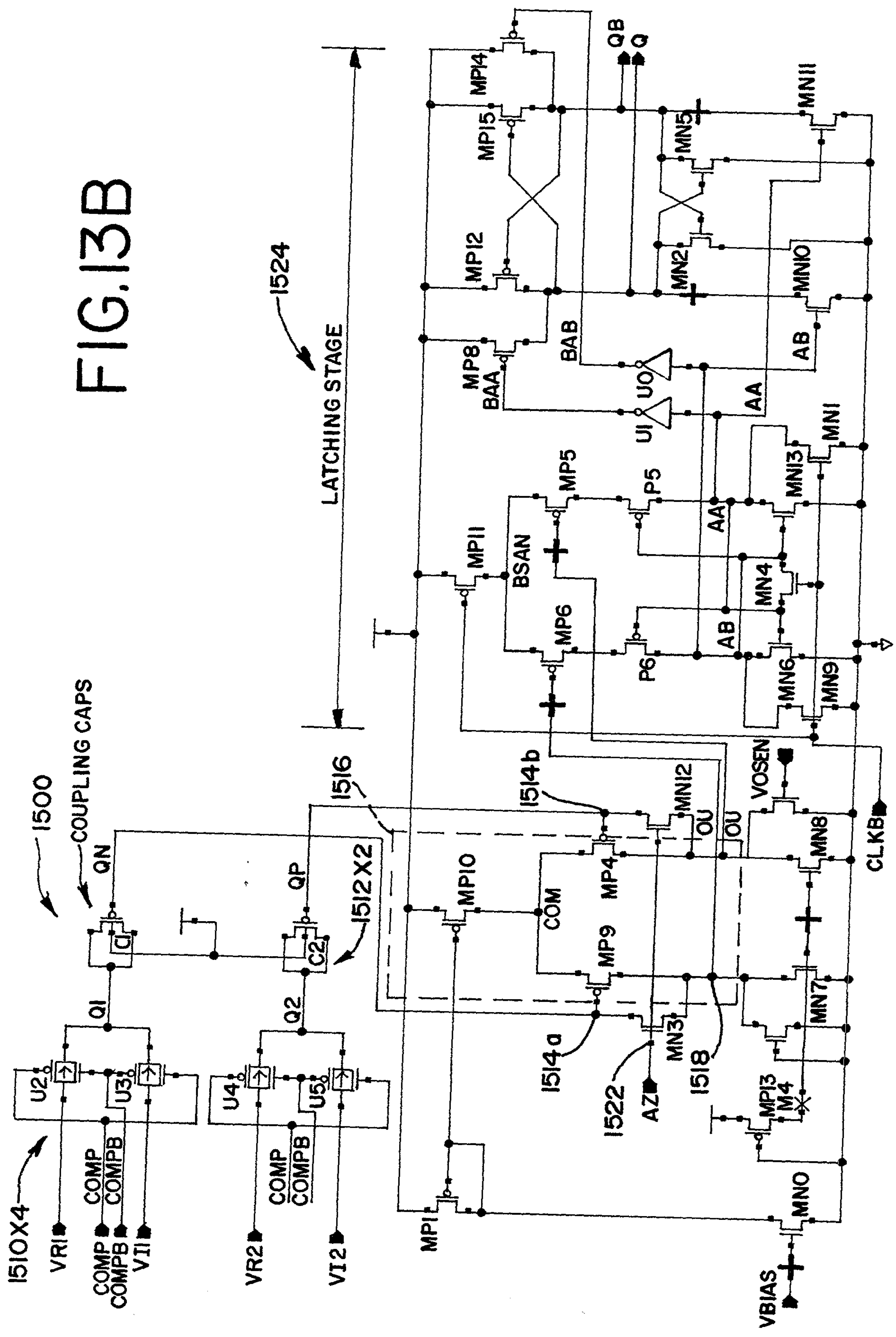

1500
COUPLING CAPS
LATCHING STAGE
1524
1510X4
1512X2
1516
1514a
1514b
1518
1522
QN
QP
Q1
Q2
C1
C2
U2
U3
U4
U5
VR1
VI1
VR2
VI2
COMP
COMPB
MP1
MP4
MP5
MP6
MP8
MP9
MP10
MP11
MP12
MP13
MP14
MP15
MN0
MN1
MN2
MN3
MN4
MN5
MN6
MN7
MN8
MN9
MN10
MN11
MN12
MN13
M4
P5
P6
U0
U1
AA
AB
BAA
BAB
BSAN
COM
OU
VOSEN
CLKB
AZ
VBIAS
QB
Q

FIG.13B

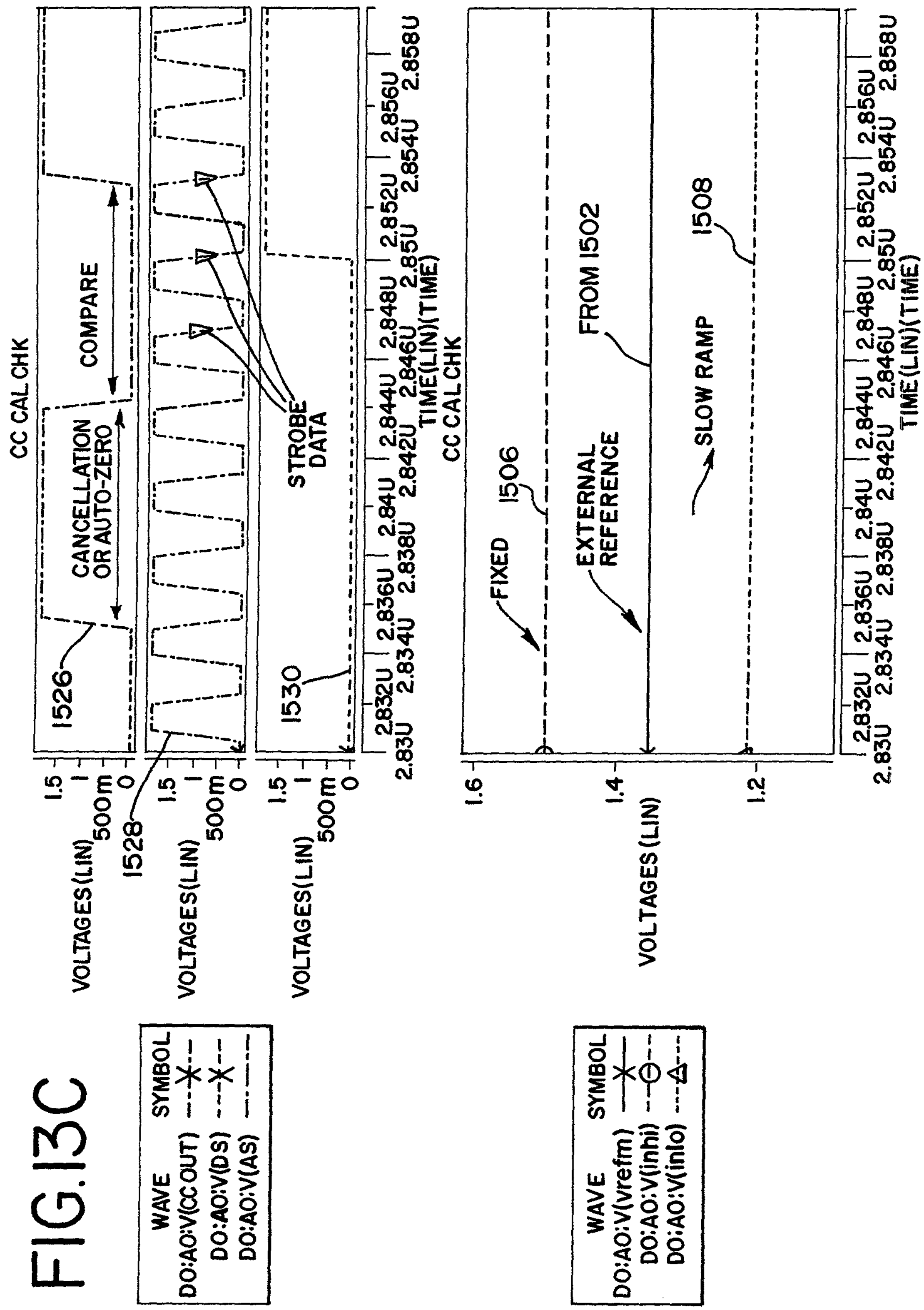

CC CAL CHK
1526
CANCELLATION
OR AUTO-ZERO
COMPARE
1528
STROBE
DATA
1530
VOLTAGES(LIN)
TIME(LIN)(TIME)
WAVE SYMBOL
DO:AO:V(CCOUT)
DO:AO:V(DS)
DO:AO:V(AS)
CC CAL CHK
FIXED
1506
EXTERNAL
REFERENCE
SLOW RAMP
FROM 1502
1508
WAVE SYMBOL
DO:AO:V(vrefm)
DO:AO:V(inhi)
DO:AO:V(inlo)

FIG.13C

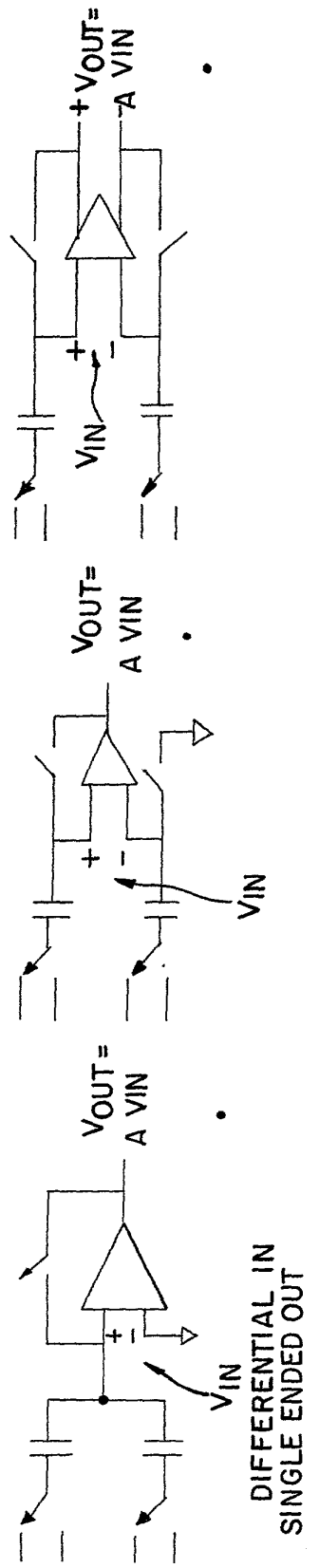


FIG. 13D

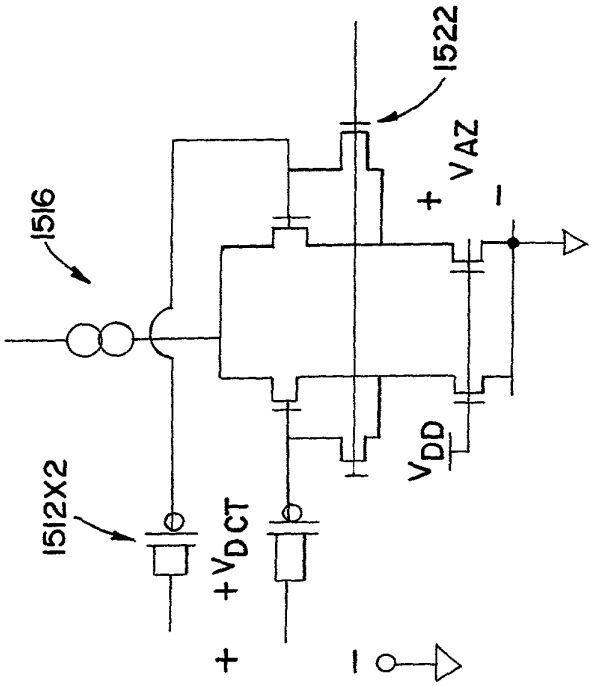


FIG. 13E

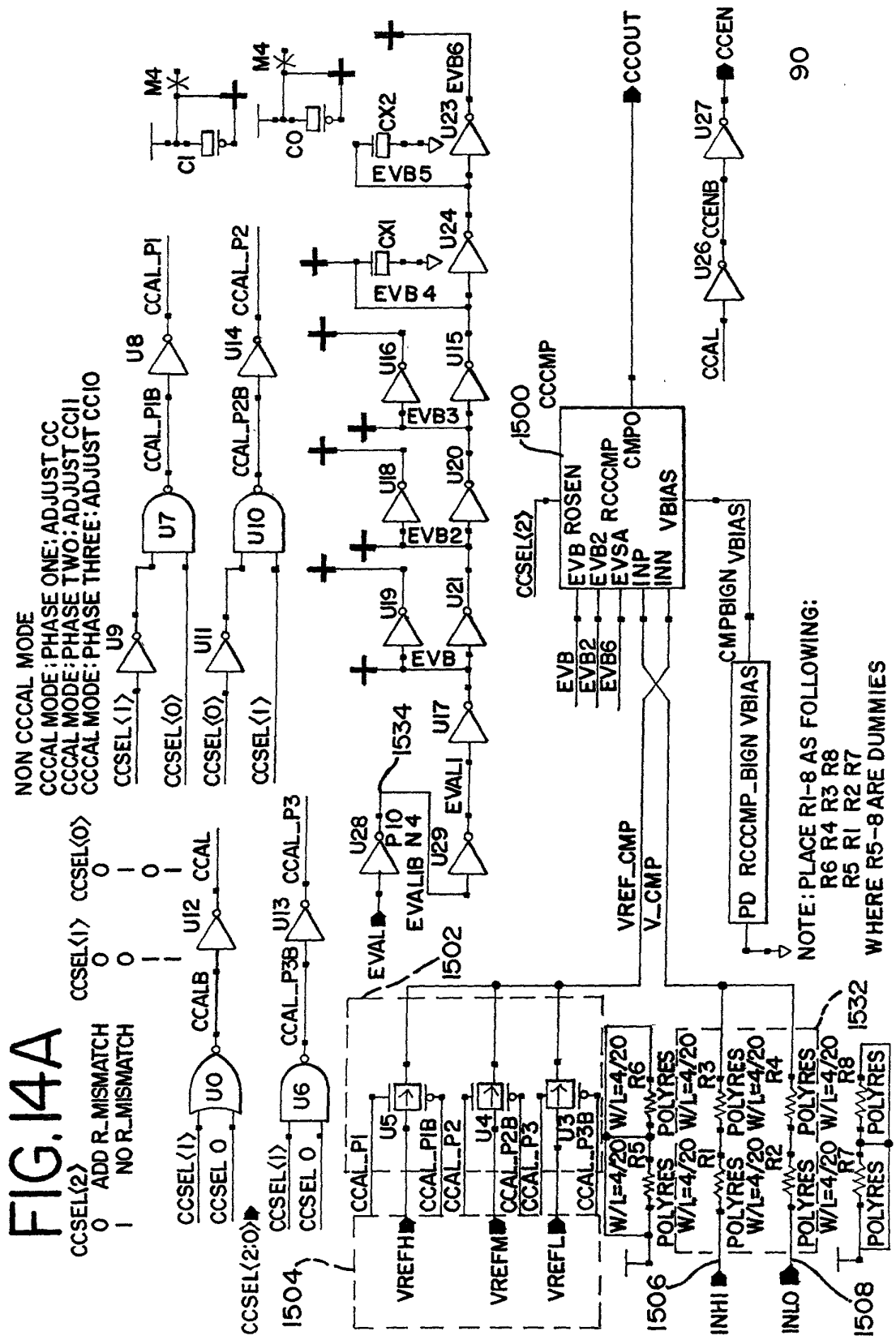


FIG. 14A
CCSEL<2>
0 ADD R_MISMATCH
1 NO R_MISMATCH
CCSEL<1> CCSEL<0>
0 0
0 1
1 0
1 1
NON CCCAL MODE
CCCAL MODE: PHASE ONE: ADJUST CC
CCCAL MODE: PHASE TWO: ADJUST CCI
CCCAL MODE: PHASE THREE: ADJUST CCIO
U0
U6
U7
U10
U11
U12
U13
U14
U8
U9
CCALB
CCAL
CCAL_P3B
CCAL_P3
CCAL_P2B
CCAL_P2
CCAL_P1B
CCAL_P1
CCSEL<1>
CCSEL 0
CCSEL<0>
CCSEL<2:0>
1504
U5
U4
U3
CCAL_P1
CCAL_P1B
CCAL_P2
CCAL_P2B
CCAL_P3
CCAL_P3B
VREFH
VREFM
VREFL
W/L=4/20
R6
R5
R1
R3
R2
R4
R7
R8
POLYRES
1506
1508
1532
INHI
INLO
EVAL
1502
EVALIB N 4
P10
U28
U29
1534
EVALI
U17
U19
U21
EVB
U18
U20
EVB2
U16
U15
EVB3
CX1
U24
EVB4
CX2
U23
EVB6
EVB5
C1
C0
M4
M4
VREF_CMP
V_CMP
CCSEL<2>
EVB
EVB2
EVB6
1500
CCCMP
EVB ROSEN
EVB2 RCCCMP
EVSA CMPO
INP
INN VBIAS
CCOUT
CMPBIGN VBIAS
PD RCCCMP_BIGN VBIAS
NOTE: PLACE R1-8 AS FOLLOWING:
R6 R4 R3 R8
R5 R1 R2 R7
WHERE R5-8 ARE DUMMIES
U26
CCENB
U27
CCAL
CCEN
90

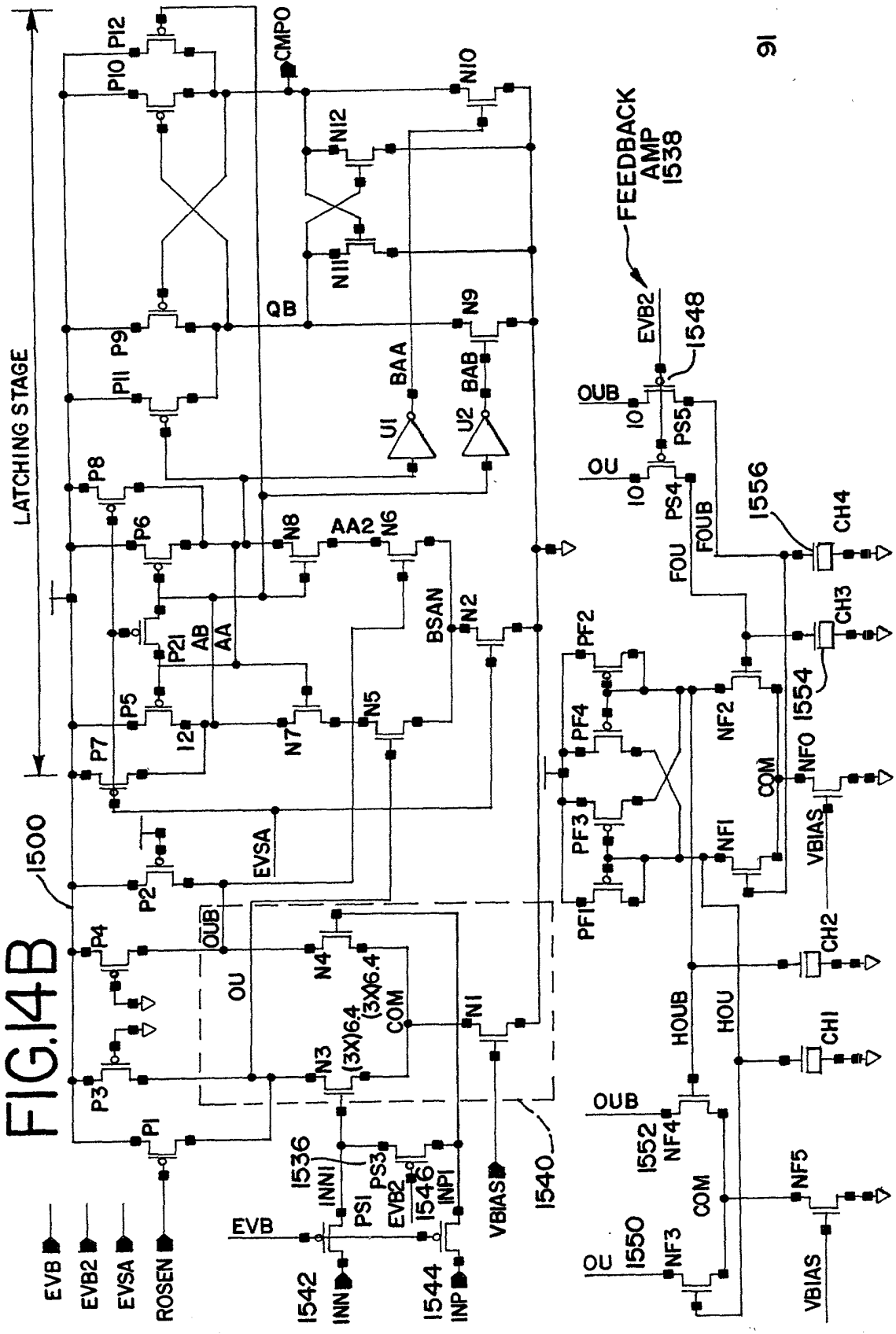

LATCHING STAGE
1500
P12
P10
CMP0
N10
N12
N11
QB
N9
P9
P11
BAA
BAB
U1
U2
P8
P6
N8
AA2
N6
P21
AB
AA
BSAN
N2
P5
P7
I2
N7
N5
EVSA
P2
OUB
P4
OU
N4
(3X)6.4
COM
N1
P3
(3X)6.4
N3
P1
1536
INN1
PS1
PS3
EVB2
1546
INP1
VBIAS
1540
EVB
1542
INN
1544
INP
EVB
EVB2
EVSA
ROSEN
FEEDBACK AMP 1538
EVB2
1548
OUB
I0
PS5
OU
I0
PS4
FOUB
FOU
1556
CH4
CH3
PF2
PF4
NF2
1554
NF0
COM
VBIAS
PF3
NF1
PF1
CH2
HOUB
HOU
CH1
OUB
1552
NF4
COM
NF5
OU
1550
NF3
VBIAS
FIG.14B
91

FIG.14C

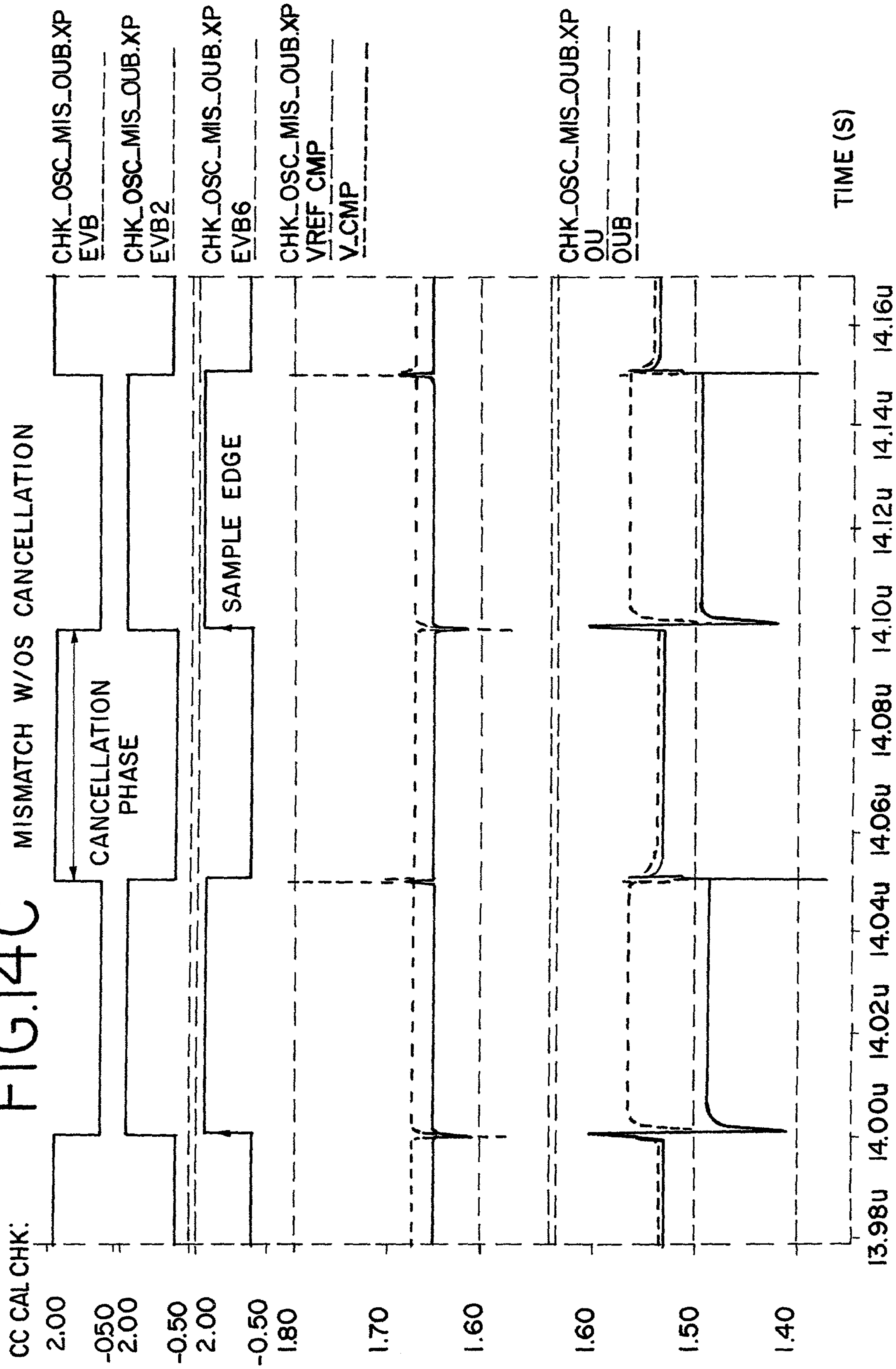

MISMATCH W/OS CANCELLATION
CANCELLATION PHASE
SAMPLE EDGE
CC CAL CHK:
CHK_OSC_MIS_OUB.XP
EVB
CHK_OSC_MIS_OUB.XP
EVB2
CHK_OSC_MIS_OUB.XP
EVB6
CHK_OSC_MIS_OUB.XP
VREF_CMP
V_CMP
CHK_OSC_MIS_OUB.XP
OU
OUB
2.00
-0.50
2.00
-0.50
2.00
-0.50
1.80
1.70
1.60
1.60
1.50
1.40
13.98u
14.00u
14.02u
14.04u
14.06u
14.08u
14.10u
14.12u
14.14u
14.16u
TIME (S)

FIG.14D

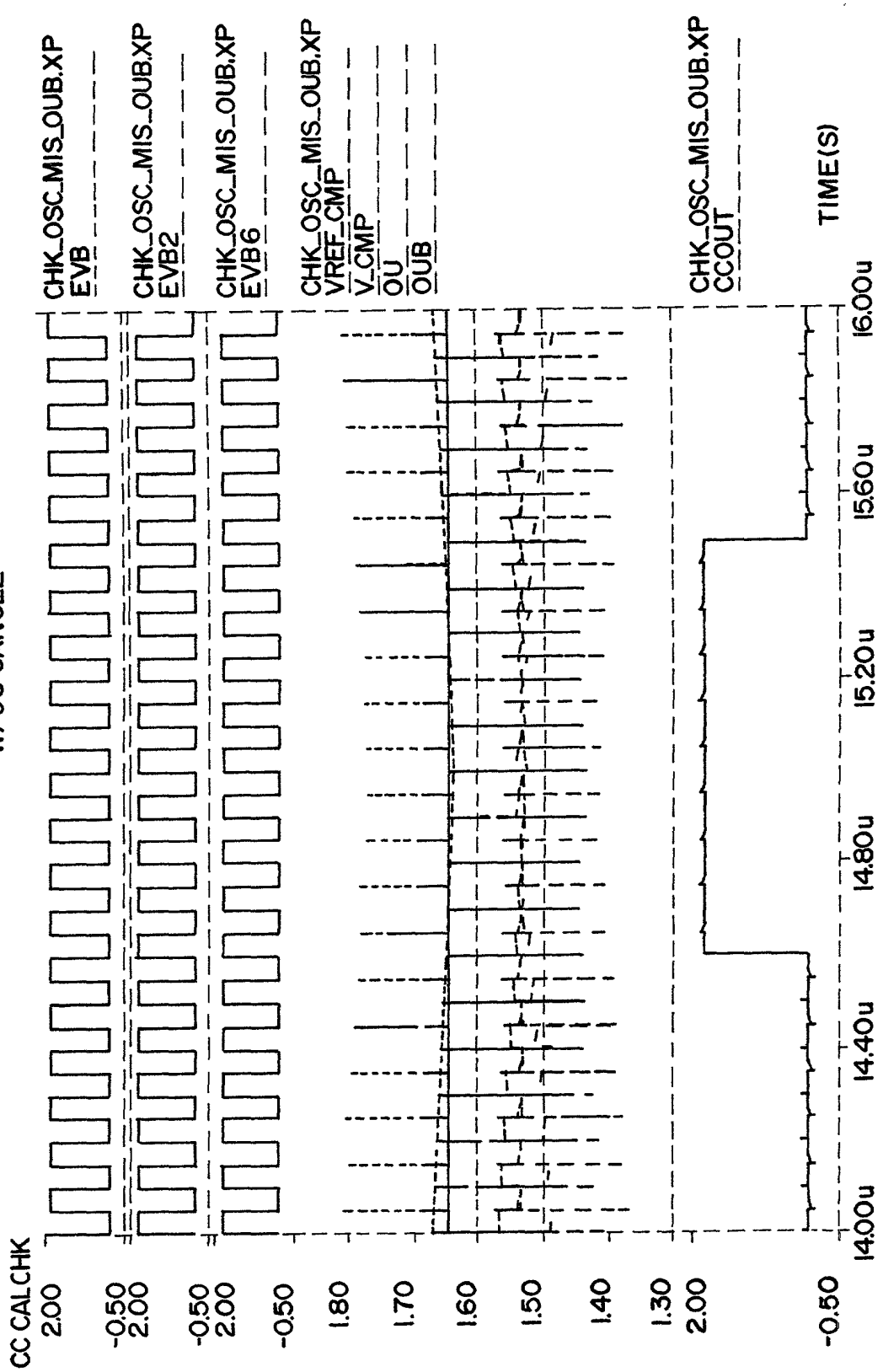


FIG.15A

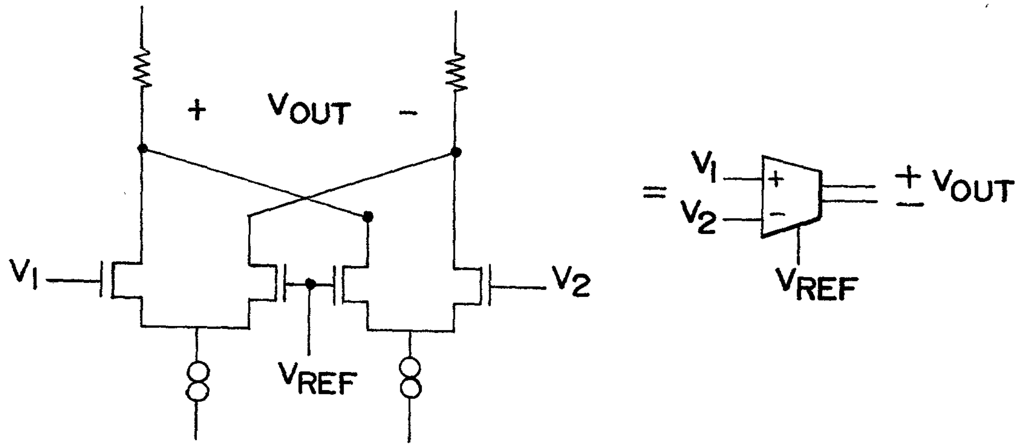


FIG.15B

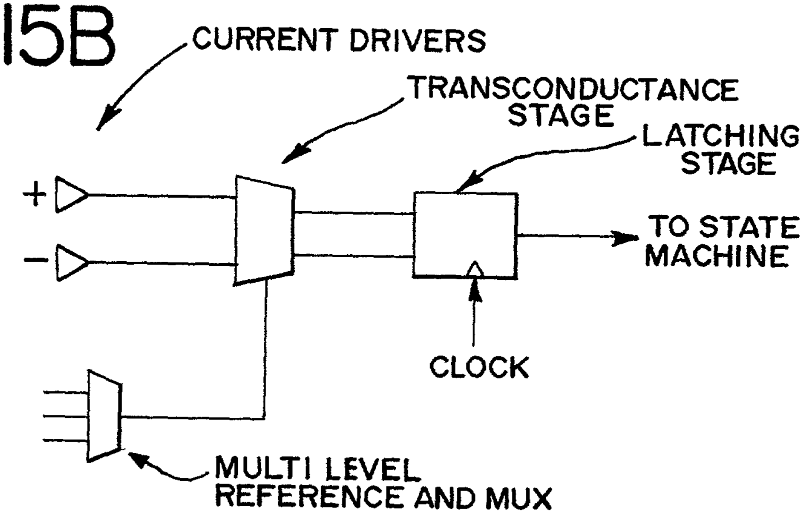


FIG.16

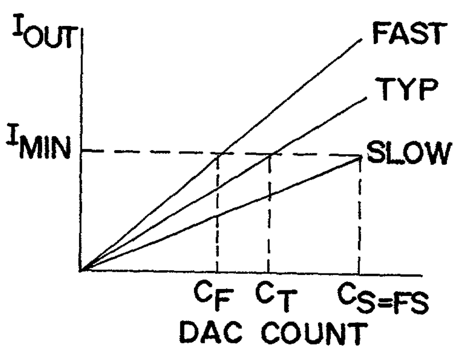
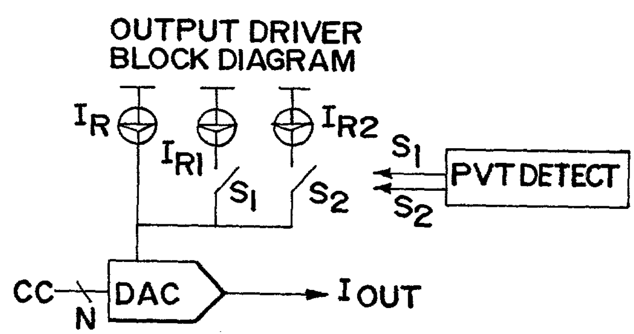


FIG.17



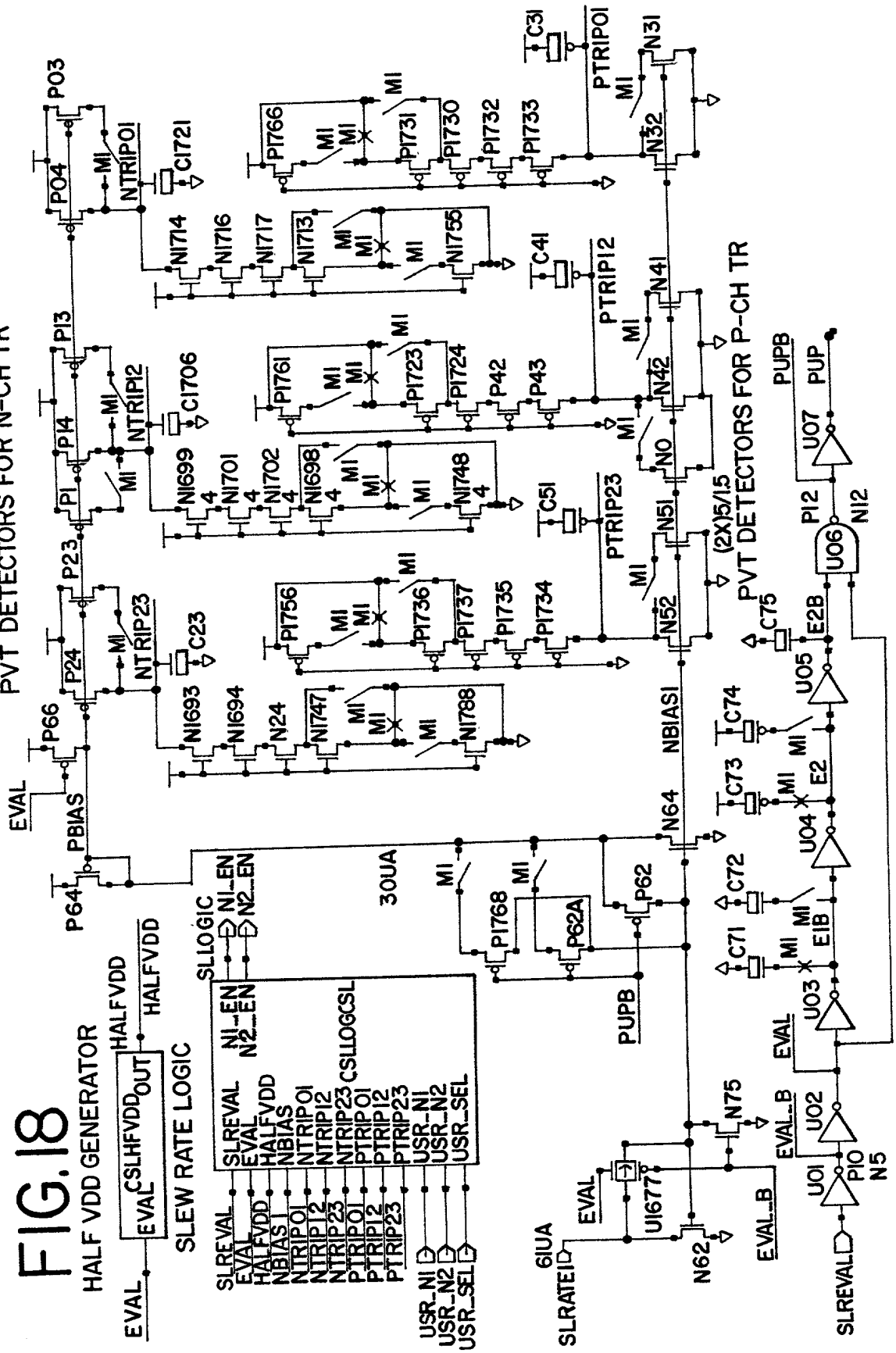

PVT DETECTORS FOR N-CH TR
PVT DETECTORS FOR P-CH TR
HALF VDD GENERATOR
SLEW RATE LOGIC
SLLOGIC
EVAL
PBIAS
HALFVDD
CSLHFVDD
SLREVAL
NBIAS1
NTRIP01
NTRIP12
NTRIP23
CSLLOGCSL
PTRIP01
PTRIP12
PTRIP23
USR_N1
USR_N2
USR_SEL
N1_EN
N2_EN
30UA
6IUA
SLRATEID
PUPB
PUP
NBIAS1
(2X)5/1.5
E2B
E2
E1B
P03
P04
P13
P14
P23
P24
P66
P64
P62
P62A
N64
N75
N62
N52
N51
N42
N41
N32
N31
N0
C1721
C1706
C23
C51
C41
C31
C71
C72
C73
C74
C75
U01
U02
U03
U04
U05
U06
U07
U1677
P10
N5
N12
P12

FIG. 18

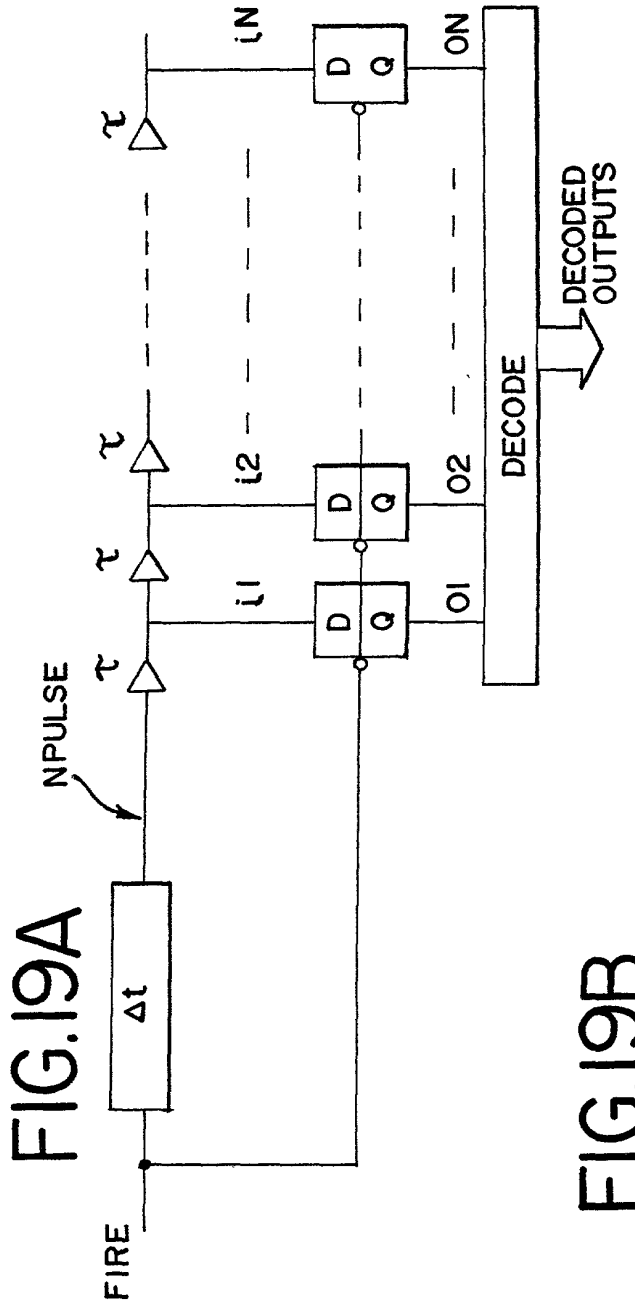


FIG.19A

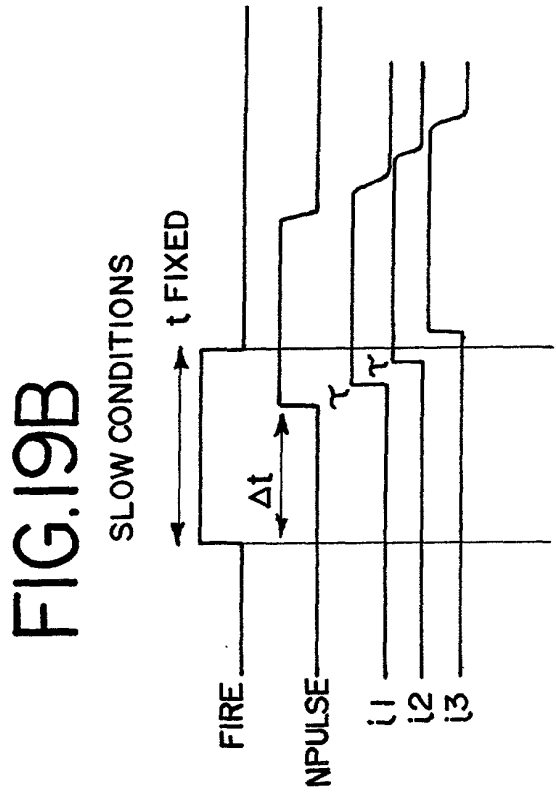


FIG.19B

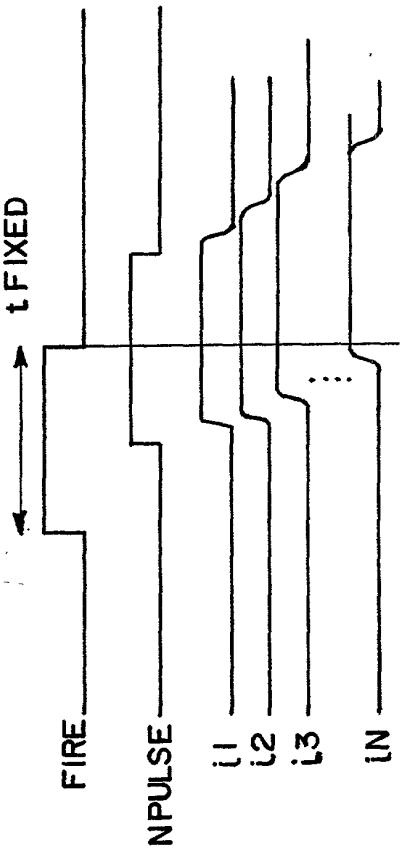
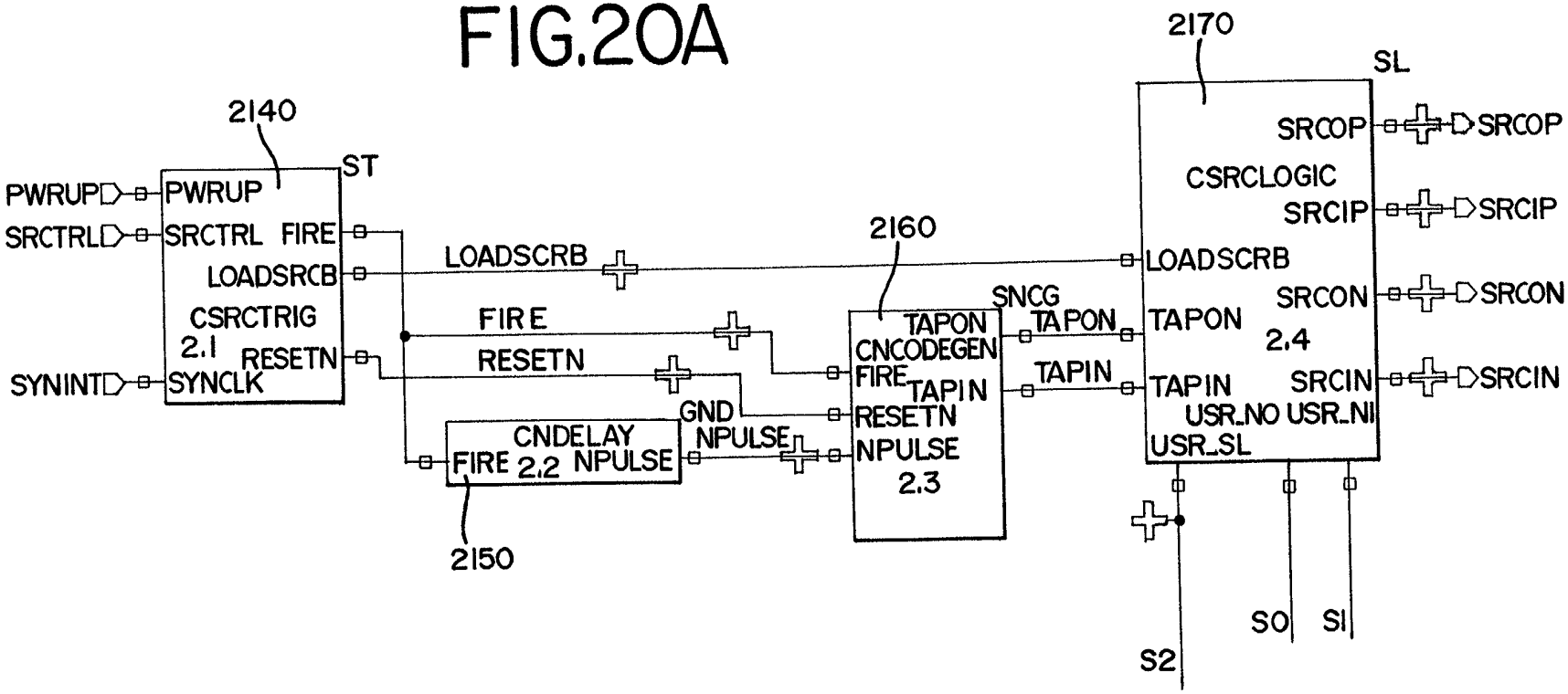


FIG.19C

FIG.20A



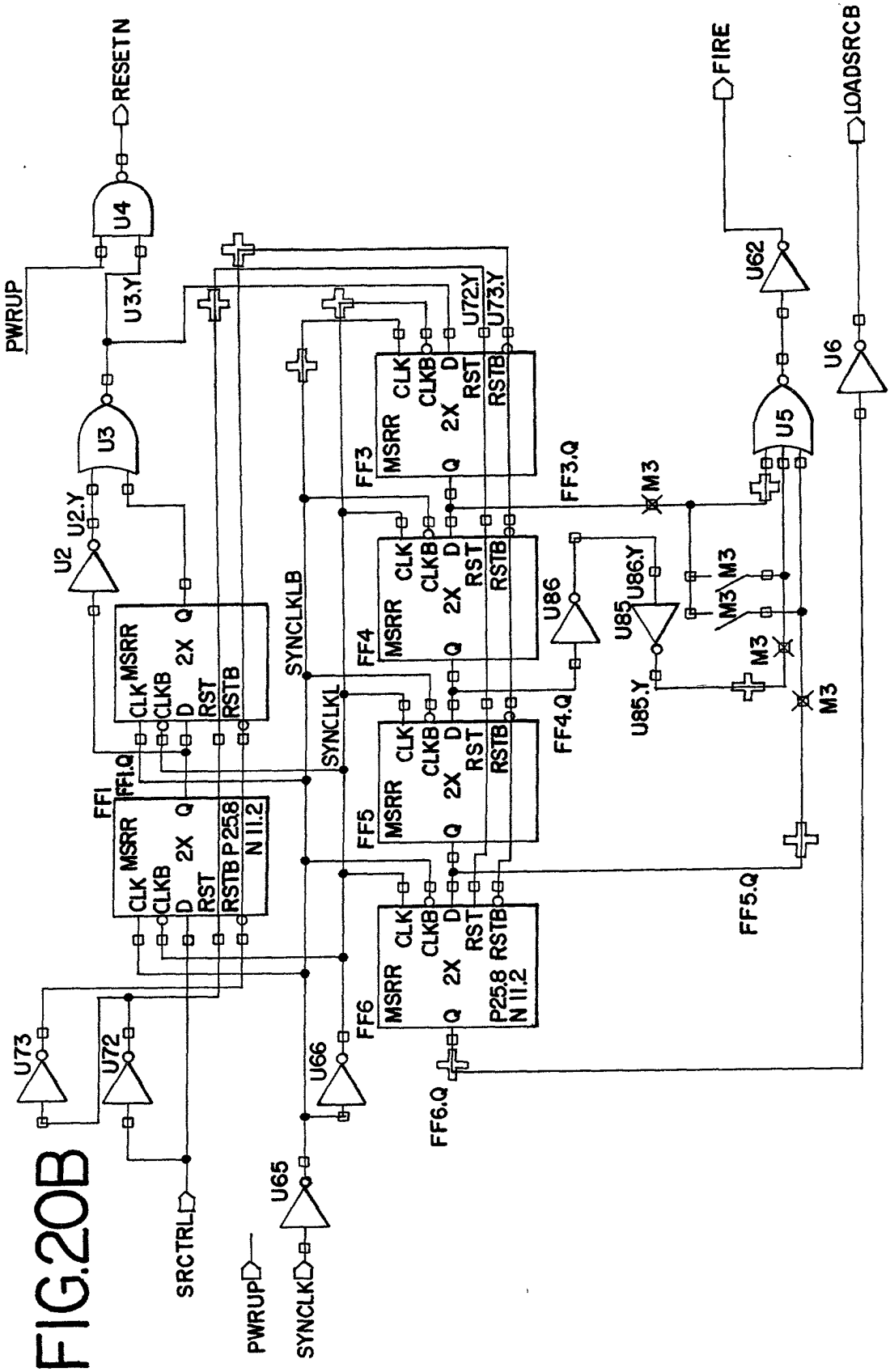


FIG.20B

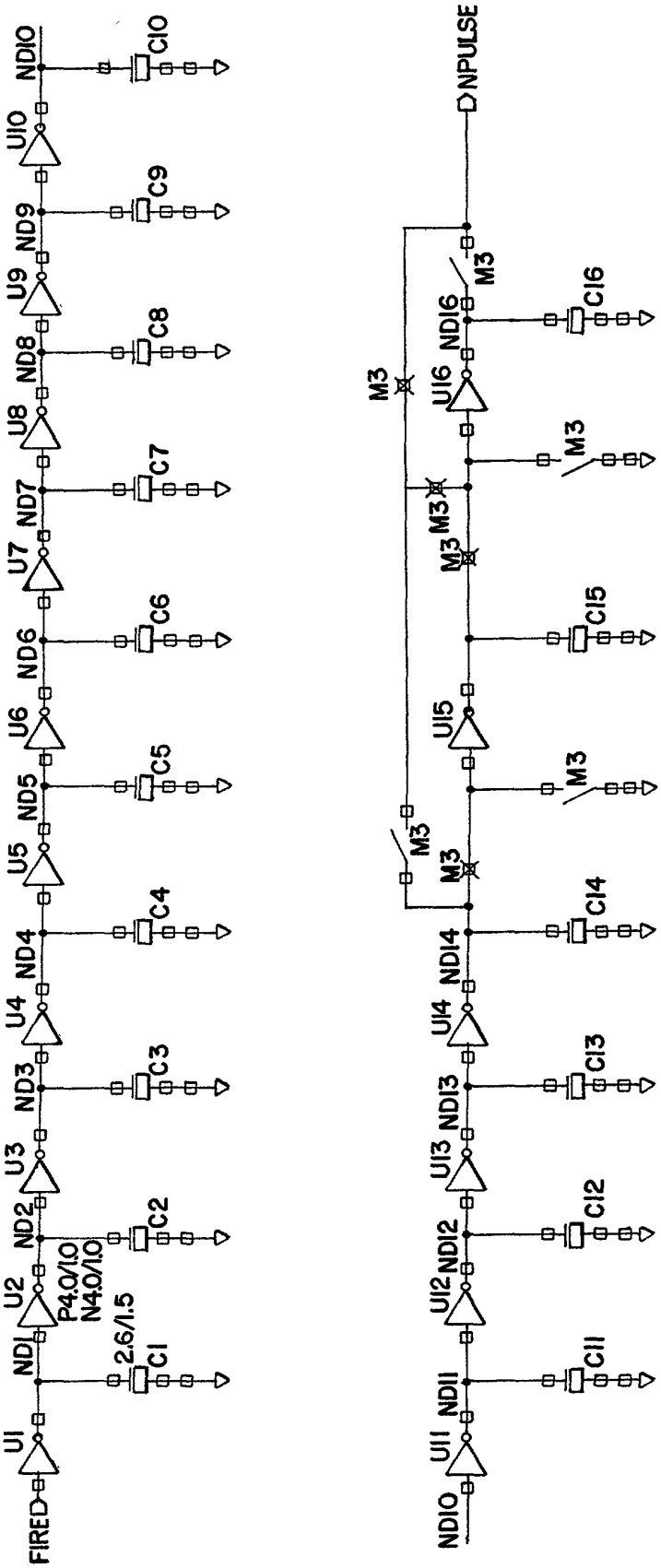

FIRED
U1
ND1
C1
2.6/1.5
U2
P4.0/1.0
N4.0/1.0
ND2
C2
U3
ND3
C3
U4
ND4
C4
U5
ND5
C5
U6
ND6
C6
U7
ND7
C7
U8
ND8
C8
U9
ND9
C9
U10
ND10
C10
NPULSE
M3
U16
ND16
C16
U15
ND15
C15
U14
ND14
C14
U13
ND13
C13
U12
ND12
C12
U11
ND11
C11
ND10

FIG.20C

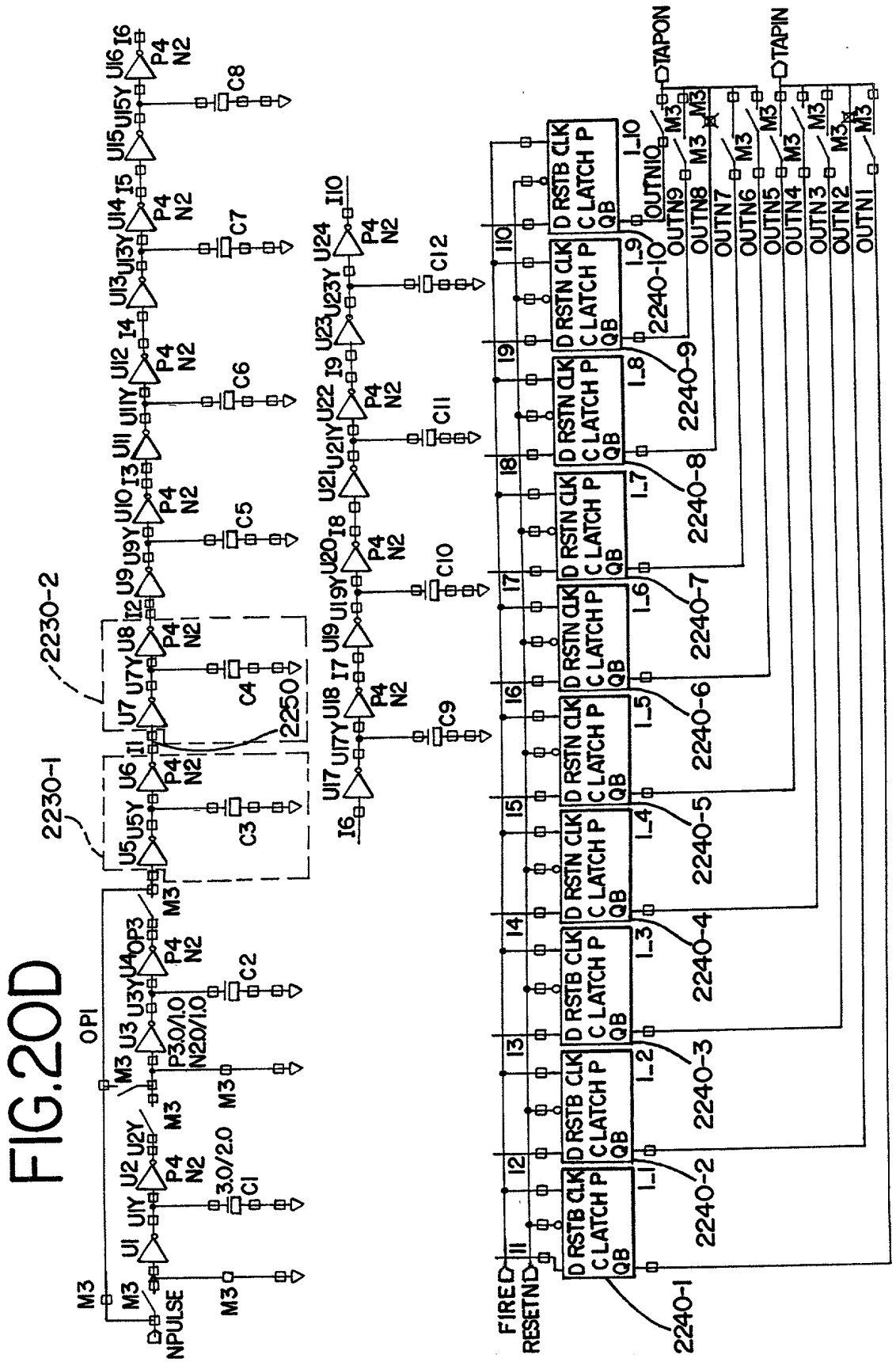


FIG.20D
NPULSE
FIRED
RESETND
OPI
2230-1
2230-2
2250
TAPON
TAPIN
2240-1
2240-2
2240-3
2240-4
2240-5
2240-6
2240-7
2240-8
2240-9
2240-10
D RSTB CLK
C LATCH P
QB
D RSTN CLK
C LATCH P
QB
P4
N2
P3.0/1.0
N2.0/1.0
3.0/2.0
M3
OUTN1
OUTN2
OUTN3
OUTN4
OUTN5
OUTN6
OUTN7
OUTN8
OUTN9
OUTN10

FIG.20E

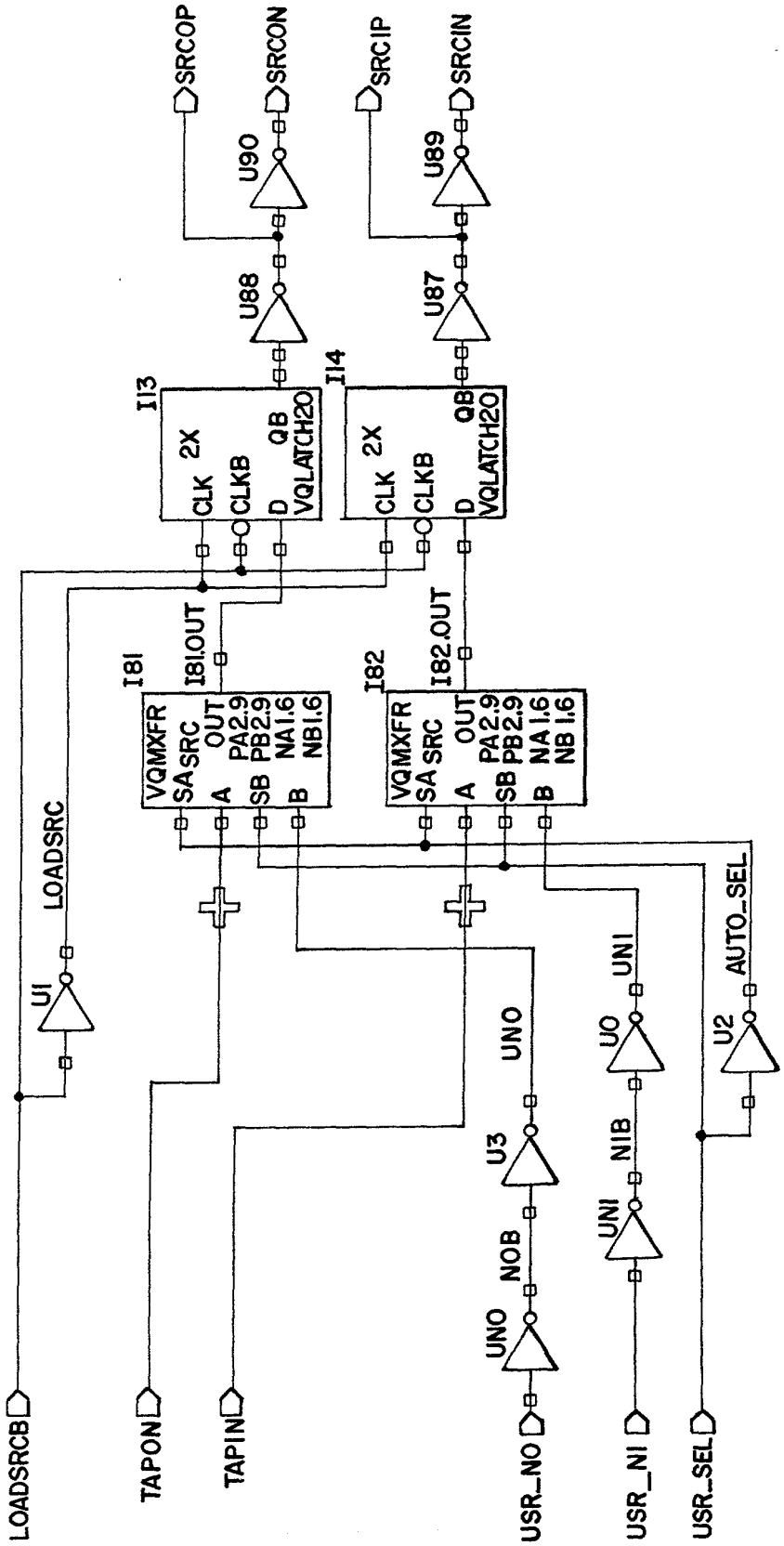


FIG.21A

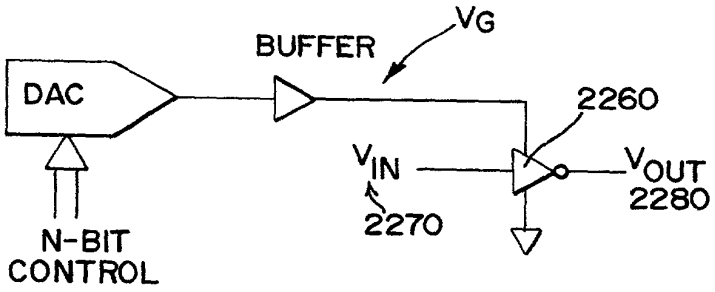


FIG.21B

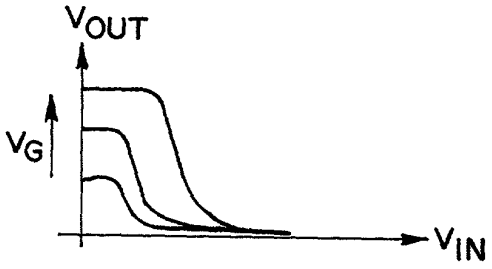


FIG.22

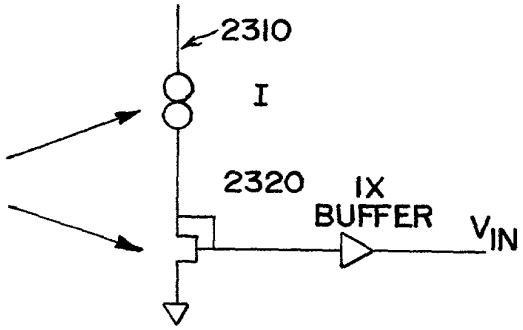


FIG.23

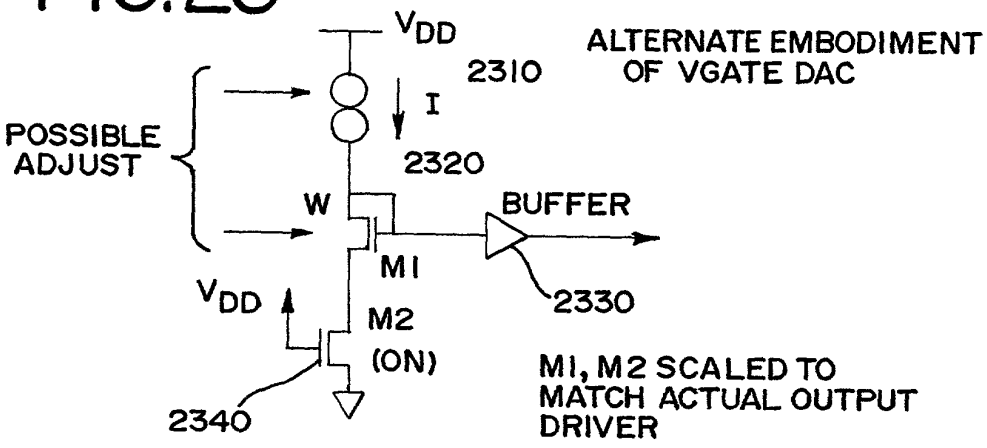
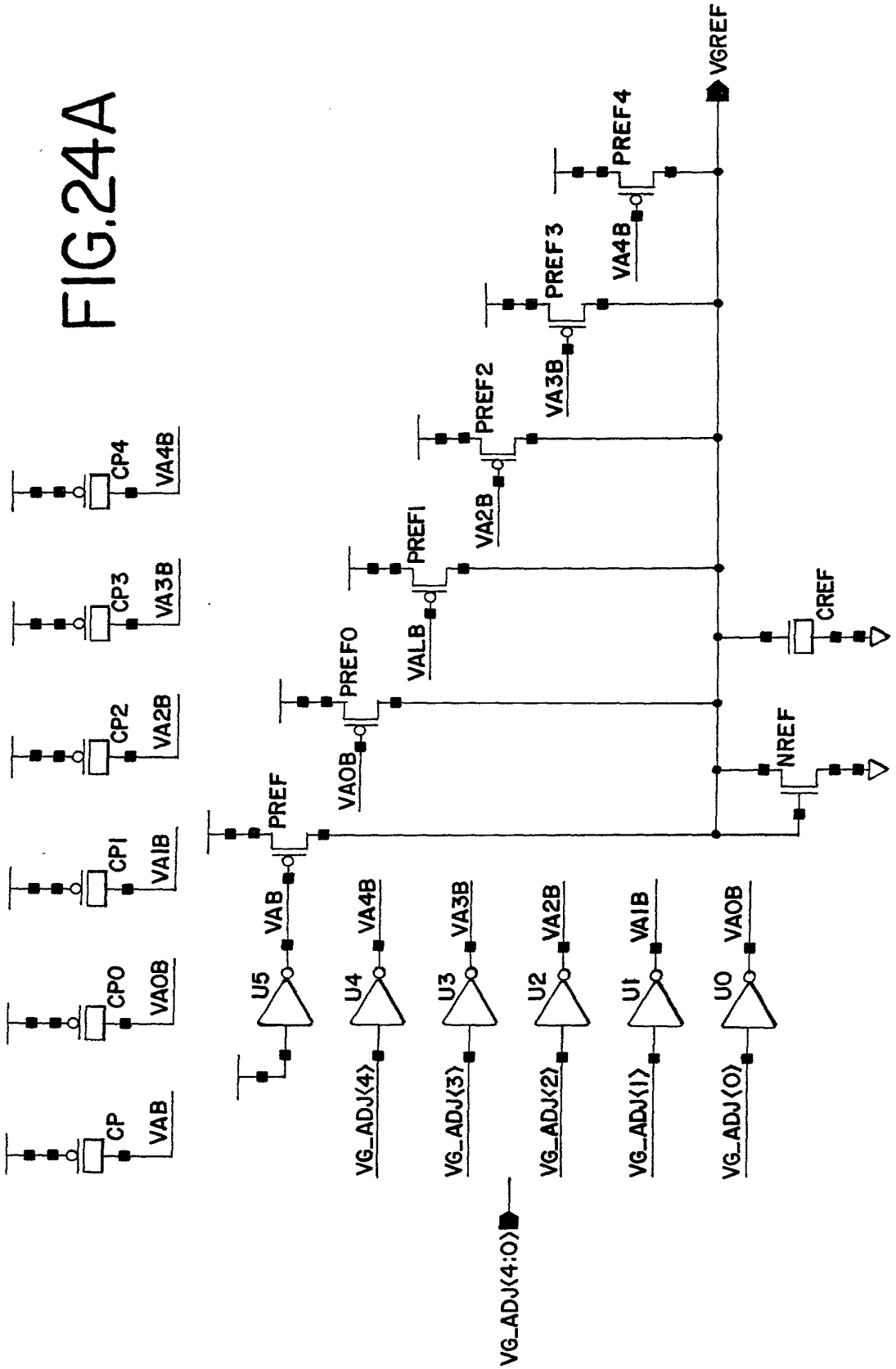


FIG.24A



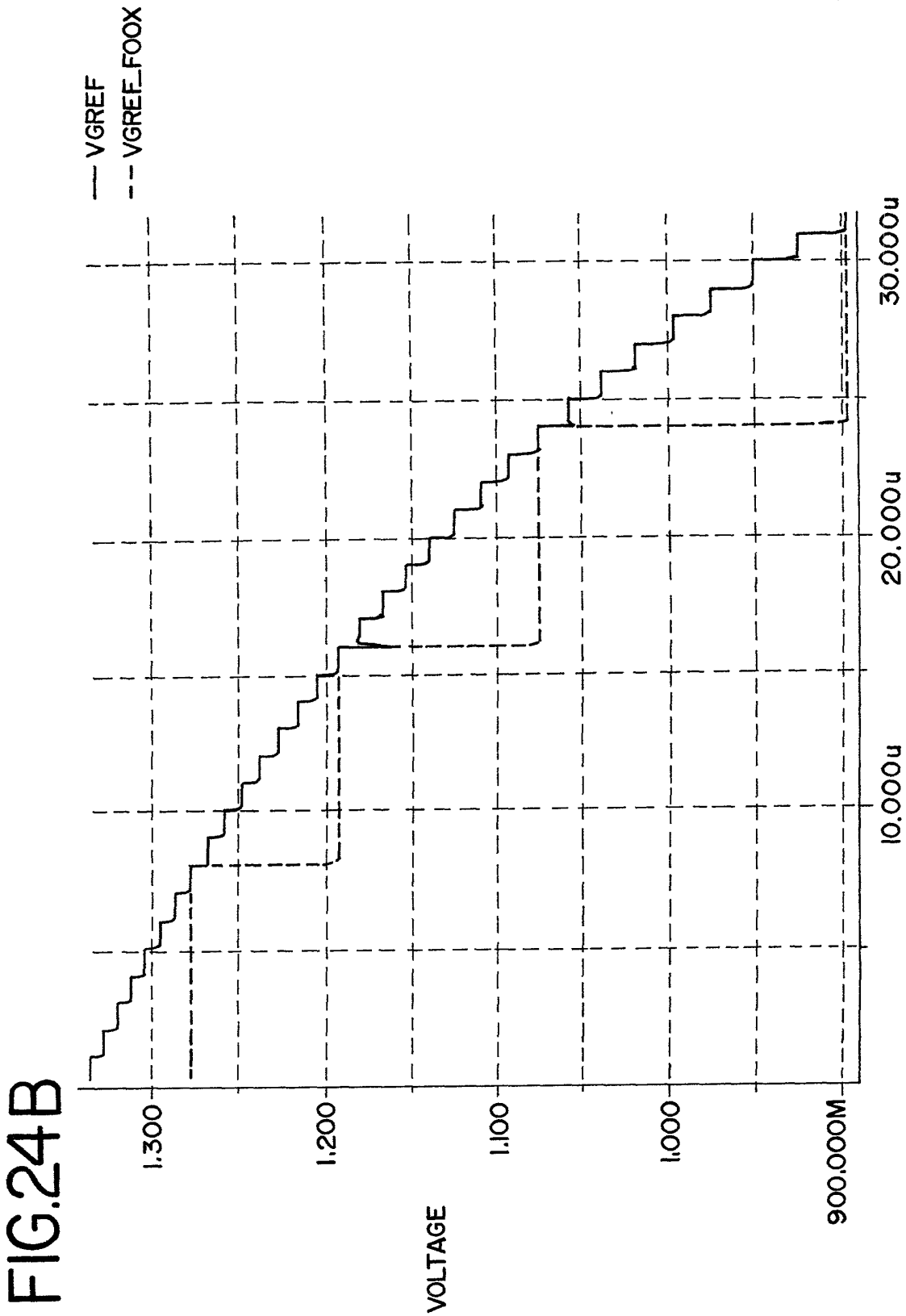

VGREF
VGREF_FOOX
1.300
1.200
1.100
1.000
900.000M
VOLTAGE
10.000u
20.000u
30.000u

FIG.24B